Raytheon

RF Vacuum Microelectronics

FINAL REPORT OPTION PHASE

29 July 1994

RAY/RD/S-5005
Contract No. MDA972-91-C-0032

Sponsored by
Advanced Research Project Agency
Defense Sciences Office

Prepared by
Raytheon Company
Research Division
131 Spring Street
Lexington, Massachusetts 02173

REPORT DOCUMENTATION PAGE

Form Approved
OMB No. 0704-0188

1. AGENCY USE ONLY *(Leave Blank)*	2. REPORT DATE	3. REPORT TYPE AND DATES COVERED
	29 July 1994	Final Technical (7/1/93 - 6/30/94)

4. TITLE AND SUBTITLE

RF Vacuum Microelectronics Final Technical Report Option Phase

5. FUNDING NUMBERS

MDA972-91-C-0032

6. AUTHOR(S)

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7. PERFORMING ORGANIZATION NAME(S) AND ADDRESS(ES)

Raytheon Company
Research Division
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8. PERFORMING ORGANIZATION REPORT NUMBER

RAY/RD/S-5005

9. SPONSORING / MONITORING AGENCY NAME(S) AND ADDRESS(ES)

Defense Advanced Research Projects Agency
Defense Sciences Office
3701 North Fairfax Drive
Arlington, VA 22203-1714

10. SPONSORING/MONITORING AGENCY REPORT NUMBER

002AD

11. SUPPLEMENTARY NOTES

12a. DISTRIBUTION / AVAILABILITY STATEMENT

12b. DISTRIBUTION CODE

13. ABSTRACT *(Maximum 200 Words)*

The results of the12 month option portion of the research and development project on high frequency Field Emission Array (FEA) cathodes is presented. Details of structure capacitance and triode operation are discussed in detail. The results did not meet the program goals and the reasons for the lack of success relative to these goals and the outlook for this technology for use at microwave frequencies are presented.

14. SUBJECT TERMS

Field Emission, Vacuum Tubes, Cathodes

15. NUMBERS OF PAGES

31

16. PRICE CODE

17. SECURITY CLASSIFICATION OF REPORT	18. SECURITY CLASSIFICATION OF THIS PAGE	19. SECURITY CLASSIFICATION OF ABSTRACT	20. LIMITATION OF ABSTRACT
Unclassified	Unclassified	Unclassified	

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Contract No. MDA972-91-C-0032

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SUMMARY

The task objective of this program was to show the feasibility of using the Field Emitter Array (FEA) cathode as a way for improved microwave tube operation. The key technical problem was to show high frequency performance from FEA cathodes. A measure of high frequency operation is the parameter F_t which is the ratio of g_m (transconductance) to C_g (input or gate capacitance) in a triode. The program goal was 1 GHz. To try to attain this goal, a variety of cathodes were fabricated and tested in a demountable high frequency test stand. The FEA cathode that gave the best results were micron sized moly tips that were fabricated in a manner similar to the standard SRI approach. The best result obtained was a value for F_t of 200 MHz. This was a measured value (not calculated for dc results) at microwave frequencies. The important technical conclusion is that g_m scales with current and there is a maximum current per tip that the FEA cathodes can operate at before self-destruction. This limits the attainable F_t to the UHF frequency regime. The significant hardware developments were two-fold; first, the design and fabrication of the FEA cathodes that operated as high as 7 microamps per tip and second the fabrication of a demountable FEA triode test stand that could operate up to 5 GHz in frequency, attain UHV vacuum operation, and could be heated to 450 degrees for device bakeout. Our conclusion from this effort is that the FEA cathode approach that was developed at Raytheon is not applicable to microwave tubes. Also, it is not clear that any of the alternative FEA cathodes that are being developed at other laboratories will work in the microwave regime.

1.0 INTRODUCTION

Vacuum Microelectronics technology is an attempt to combine the best features of low cost solid state fabrication techniques and vacuum tube electronics. One goal is the development of cathodes that can be modulated at the carrier (not a modulation) frequency. This concept has worked well at UHF frequencies with gridded cathodes to reduce tube size and increase efficiency. To push this concept up into the microwave frequencies requires a new technology. This is because the small grid spacings required cannot be manufactured with conventional tube technology. The new technology is micron-sized gated field emission cathode arrays. The program goals were to fabricate triode structures that met the following criteria:

1. $F_t = g_m/2\pi C_g > 1$ GHz
2. $V_g < 250$ volts
3. $J > 5$ A/cm^2
4. $I > 5$ mA

The nomenclature for the triode's ports is a mixture of solid state FET and tube terms. The electrons start from the field emitter cathode (source) are modulated by the gate (grid) and are collected by the anode (drain).

The first criteria (F_t) is the ratio of the small signal transconductance (g_m) to the gate capacitance (C_g). This a measure of the maximum operating frequency of the triode. The second criteria V_g is the gate voltage required to obtain the g_m in the first term and J and I in the following terms. J is the current density and I is the total current at the operating point. The operating life had to be at least one hour. The anode voltage, pulse width and duty cycle were not specified.

The goals were not all met in this option phase of the contract. The best results are listed below:

1. F_t = 0.2 GHz
2. V_g = 154 Volts
3. J = 37 A/cm^2
4. I = 7.3 mA

   Anode voltage = 500 volts, pulse width = 1 ms, duty = 4%

The F_t goal was not met. This is because g_m scales with current and there is a maximum current the cathodes will operate before destruction.

Section 2 presents device layout and capacitance calculations and measurements of the cathodes. Section 3 presents the triode configuration and the test results of the best triode. Section 4 briefly covers the attempts to reduce the work function of the tip through coatings. Section 5 concludes with suggestions for future work.

2.0 DEVICE DESIGN

2.1 Layout

The cathode for the triode is made using the standard "microtip" processing. The details of the process steps were documented in the final report of the basic part of contract MDA972-91-C-0032. The cathode substrates were sapphire. Two new chip designs were made for this option phase of the program. The first design is shown in Figure 2-1. It has of two sets of identical structures along each edge with test structures in the interior. The edge structures have bonding pads to connect to the alumina for hot test while all the devices have probe pads for RF cold test with microwave probes. During phase one of the contract, it was noticed that sometimes there was stray emission from the bond wires during operation. Therefore a second chip design shown in Figure 2-2 was made. In this layout, the cathode is moved away from the bonding pads by extending the co-planar line into the interior. To do this all the cold test structures were removed. On both designs the outer pitch for external connections is 300 microns while the inner pitch for on-wafer probing is 100 microns. The connections are all ground-signal-ground.

An accurate measurement of the capacitance is required for calculating F_t. The measurement should be done at the operating frequency (1 GHz). Therefore, the calibration of the vector network analyzer is important. On wafer RF probing techniques have become routine in the MMIC industry in the microwave regime. As a check on the calibration, an open and a short should be included in the die. These are shown in Figures 2-3 and 2-4 respectively.

Two cathode configurations were used. The "dense" configuration is shown in Figure 2-5. It consists of 400 microtips (20 x 20) on a 3 micron pitch inside a 70 micron square gate shown in Figure 2-6. The "under dense" configuration consists of a 5 x 5 array of sub-cathodes each on a 28 micron pitch. Each sub-cathode

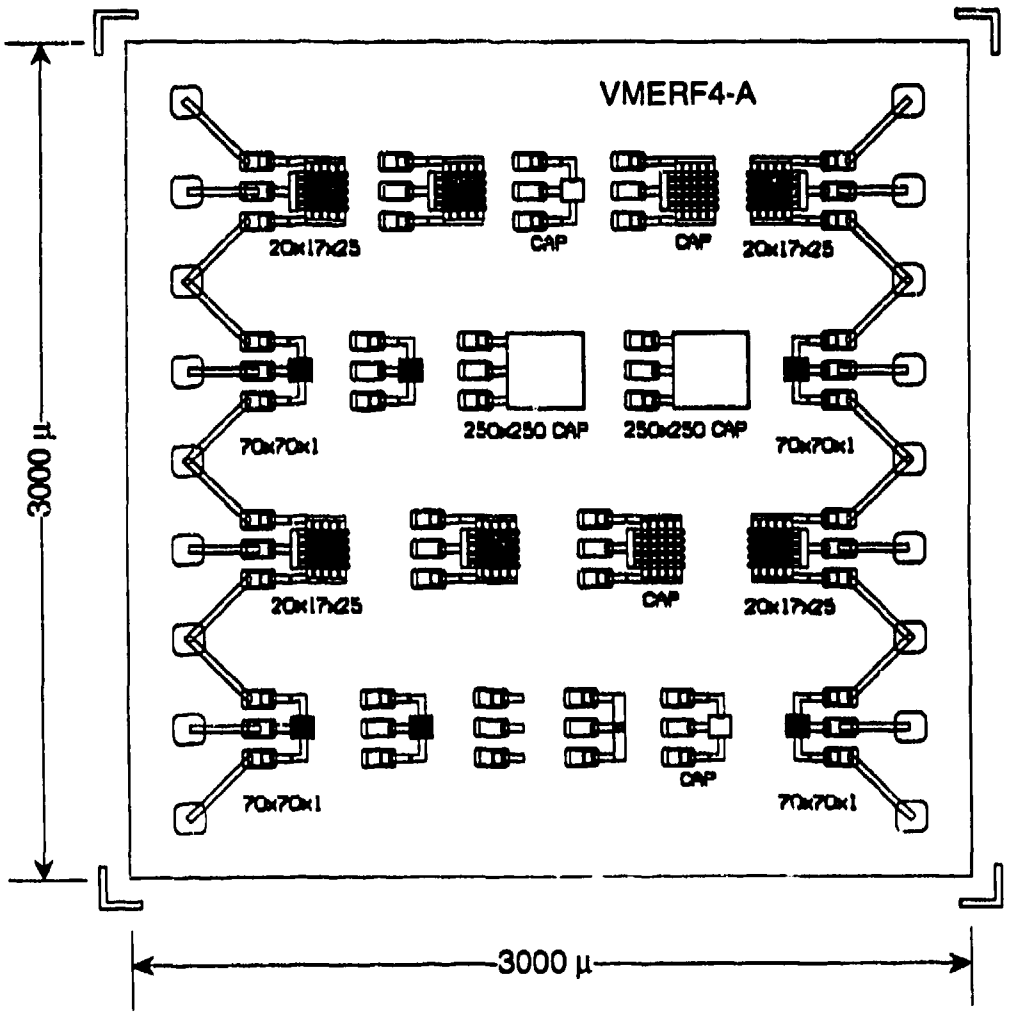

Figure 2-1. Chip Design 4A - Test and Short Lead Devices.

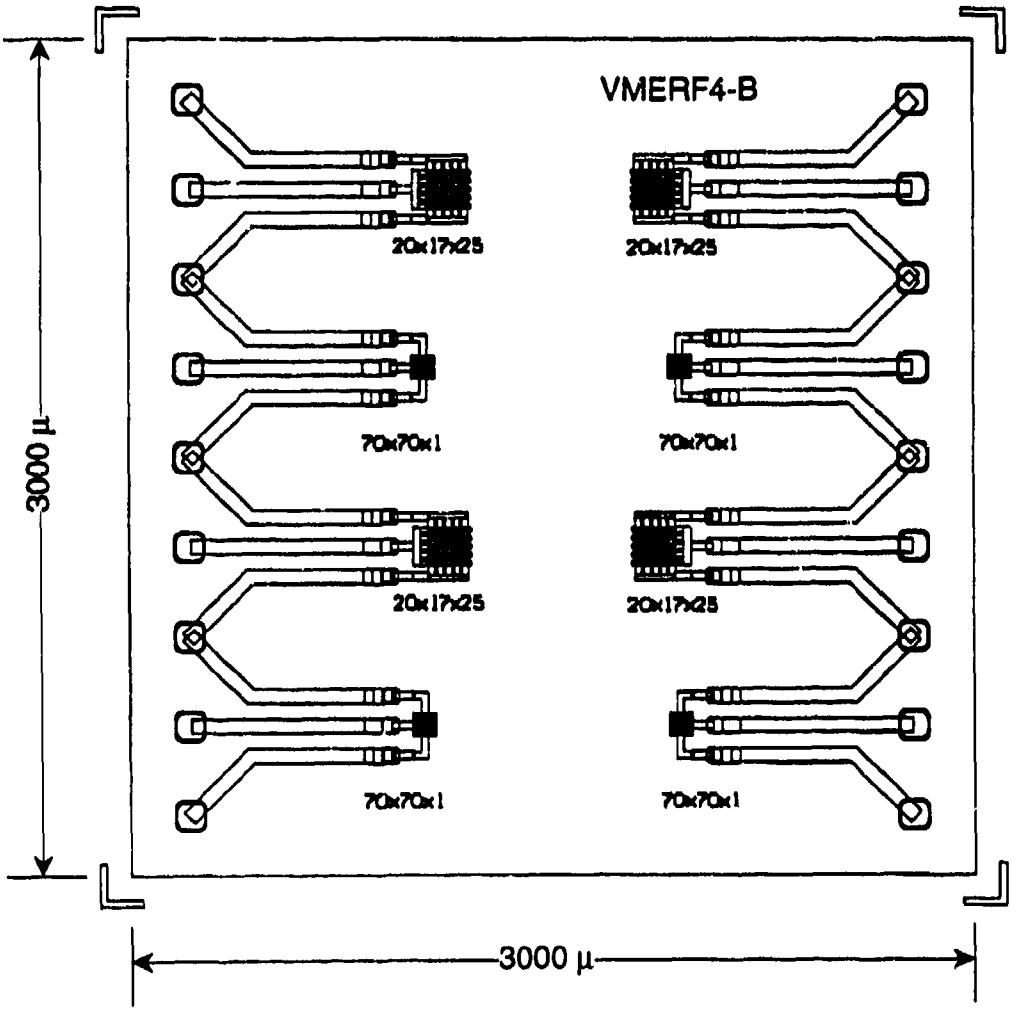

Figure 2-2. Chip Design 4B - Long Lead Devices.

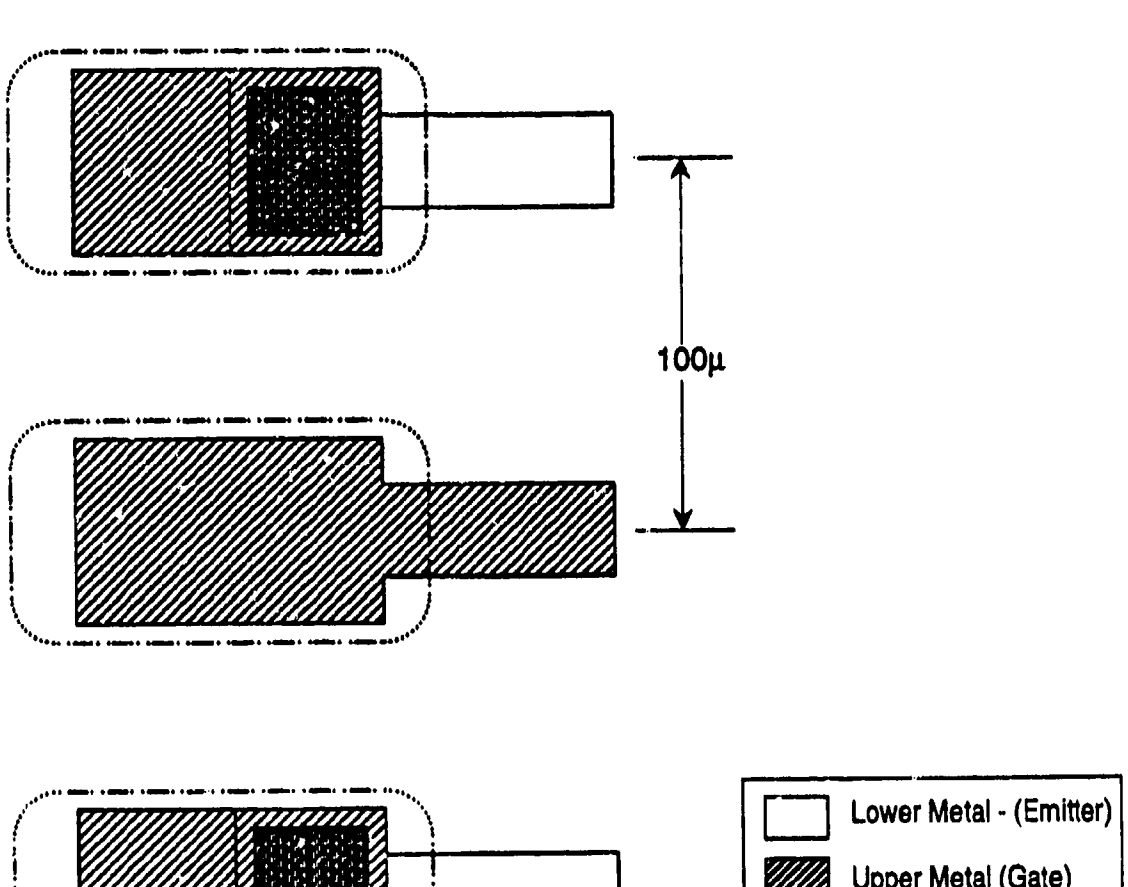

Figure 2-3. RF Calibration Open.

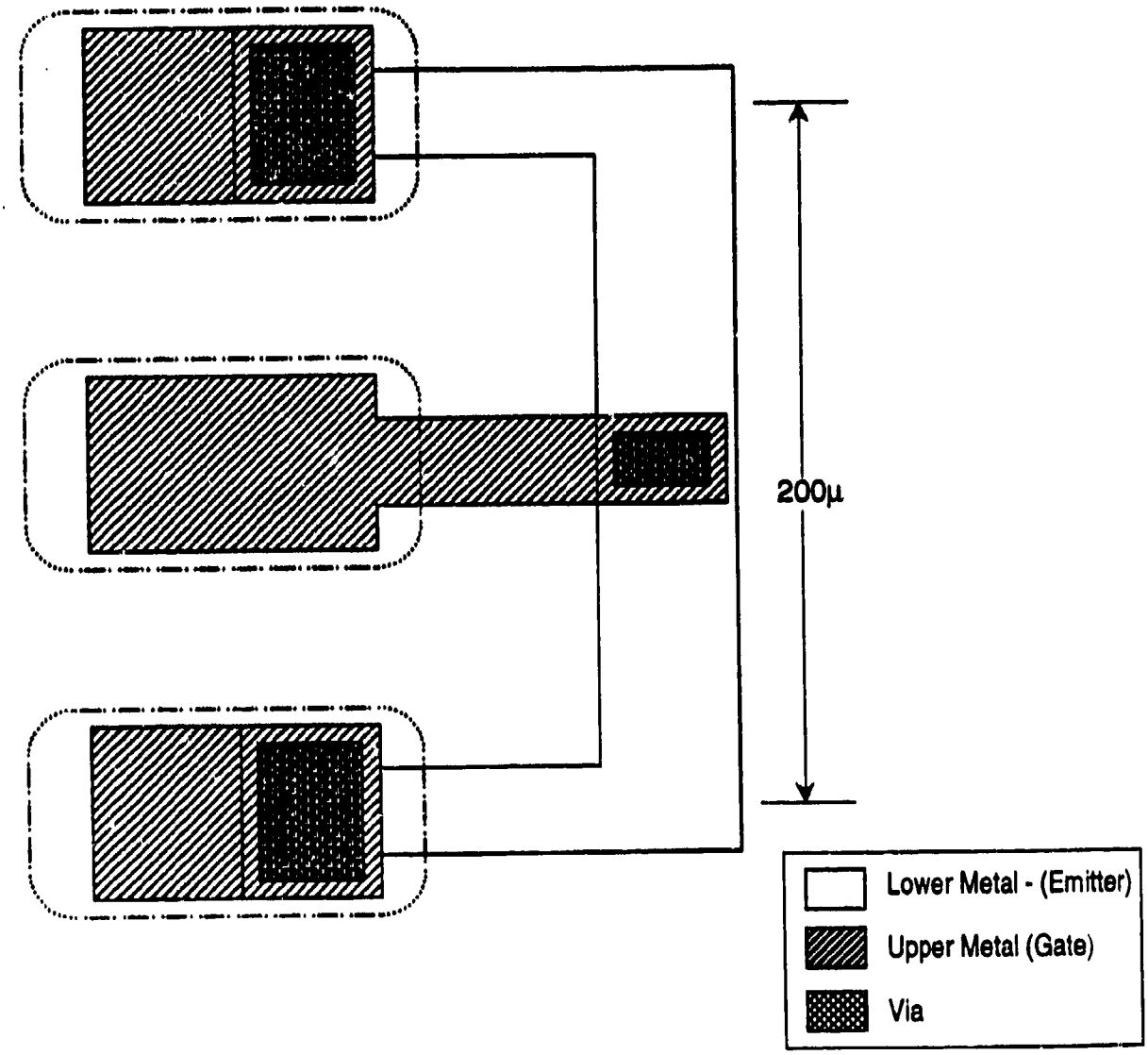

Figure 2-4. RF Calibration Short.

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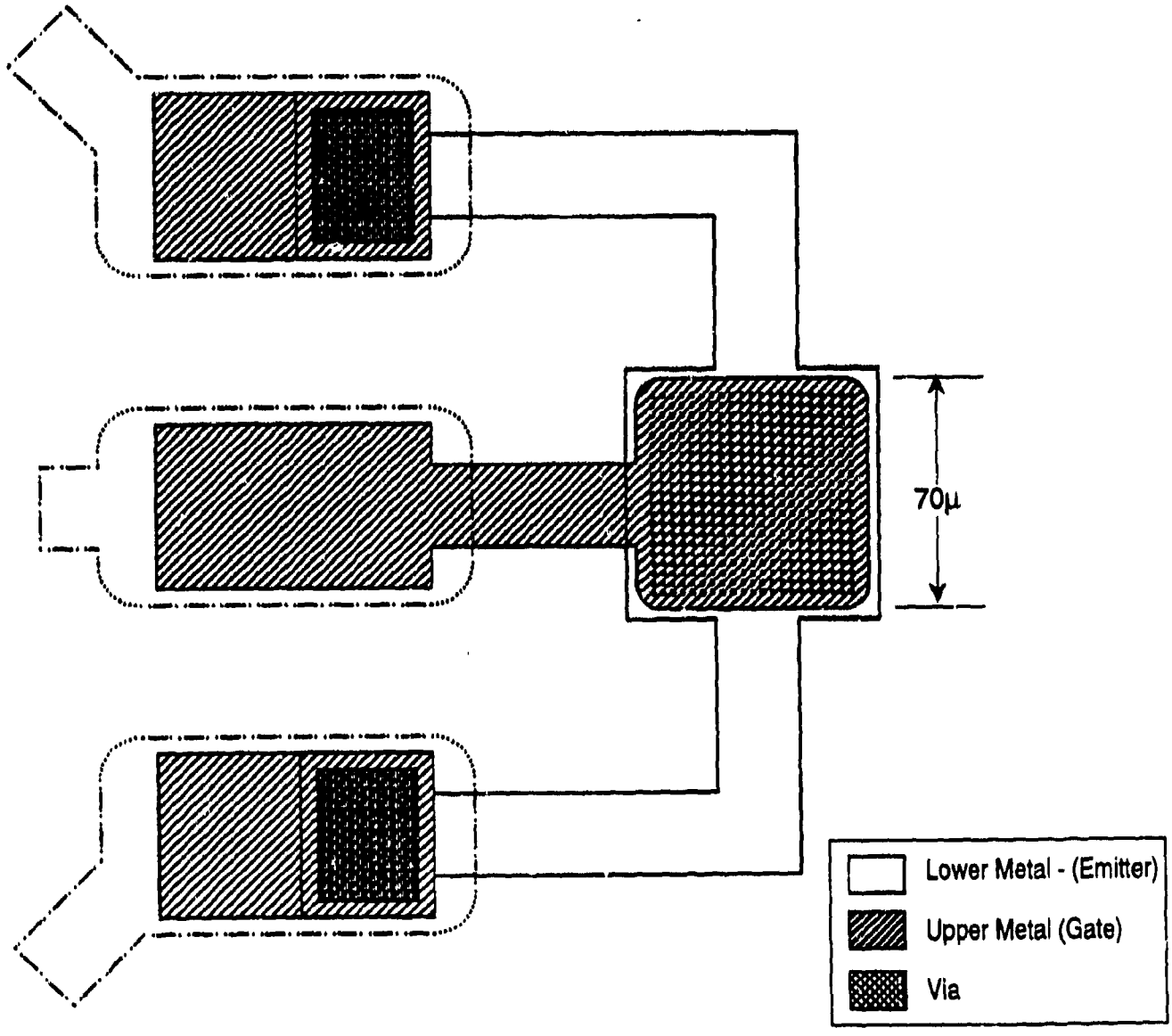

Figure 2-5. Dense Device Structure Layout (400 tips).

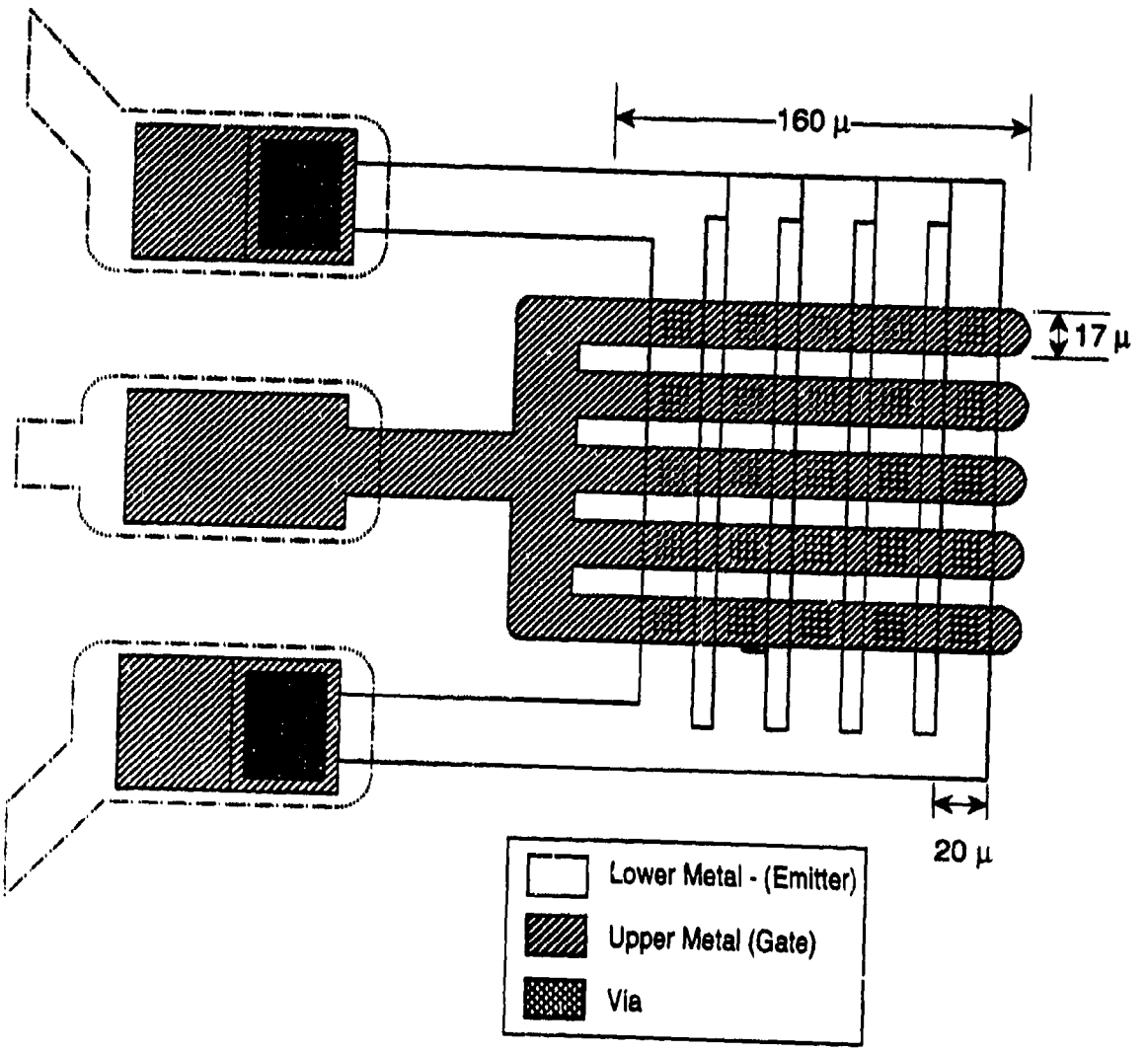

Figure 2-6. Under Dense Device Structure Layout (400 tips).

consists of 16 microtips (4 x 4) on a 3 micron pitch inside a 17 x 20 micron gate. The edge of the "under dense" layout was about twice that of the "dense" device. The dense structure has a high number of tips per unit area and therefore if all the tips emitted uniformly, the higher F_t. The problem is running such a dense structure to high currents. Any arc that occurs can travel across the whole cathode. The second design will have a better ability to quench an arc at the sub-cathode boundary. This topology is similar to that found in the French LETI/PIXEL cathodes. In practice we found that the higher currents that could be obtained from the "under dense" structure more than made up for the increased capacitance.

2.2 Gate Capacitance

The capacitances of the cathode not including the tips calculated and compared to measurements. The nominal emitter to gate spacing is 1 micron with the dielectric constant of the SiO_2 of 3.7. The calculations were performed using the Hewlett Packard product HFSS (high frequency structure simulator). A three-dimensional view of the dense structure is shown in Figure 2-7 and a zoom of the detail is shown in Figure 2-8. By the symmetry of the device, a magnetic wall is used on the left to reduce the computational array by one-half. The bottom half is the dielectric substrate and the top is air. The box had to be made much larger than the device to reduce to stray capacitance of the box to a value small compared to the device capacitance. The full box and a zoom of the under dense structure is shown in Figures 2-9 and 2-10 respectively. The results of a simple parallel plate calculation, the full three-dimensional simulation and the on wafer measurements are tabulated in Table 2-1. The dense structure results are quite good. As expected, the measured and simulated agree and are higher than the parallel plate. The under dense results show the same trends, however the three-dimensional simulation is a factor of two too high. We postulated that the HFSS product has a problem with the closely packed fringing fields of the under dense structure. This on wafer measured value of 0.345 pf was used in calculating the F_t of this device.

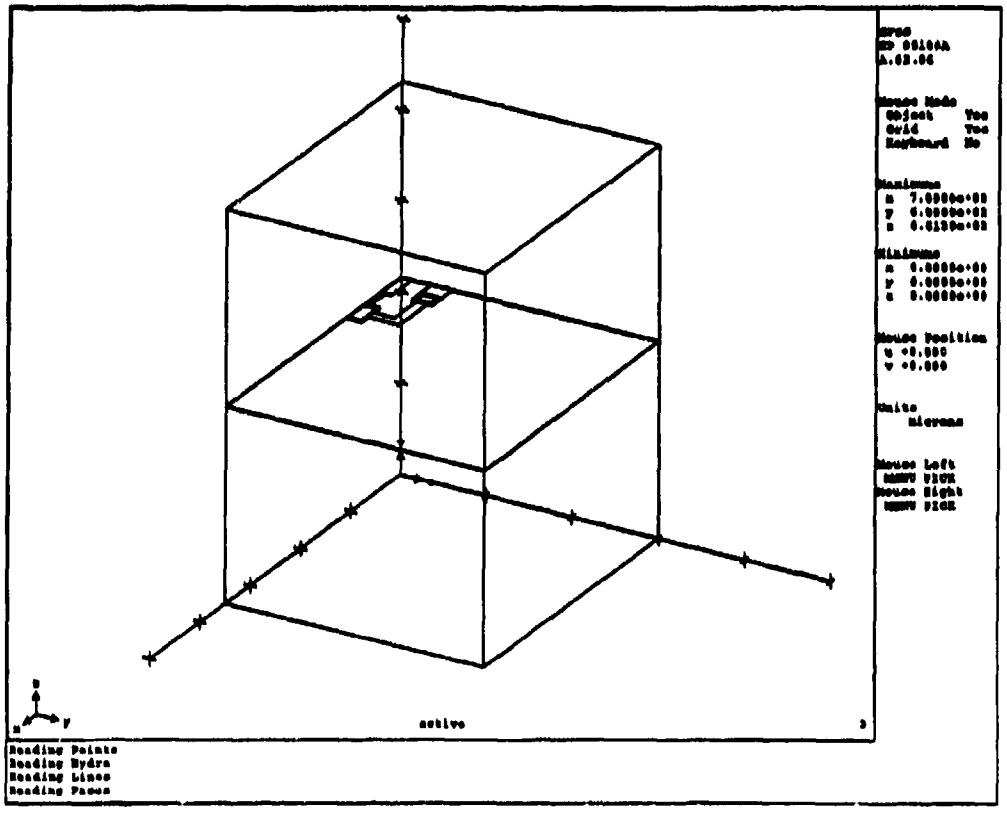

Figure 2-7. Dense Structure Simulation - Full View.

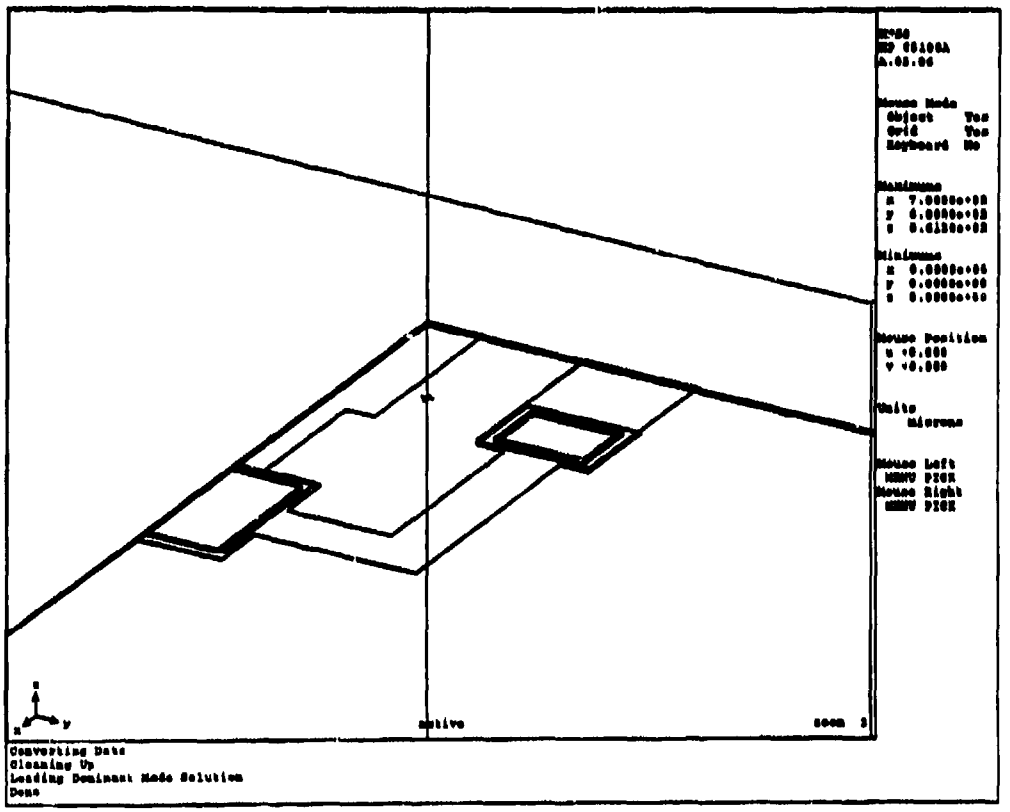

Figure 2-8. Dense Structure Simulation - Zoom.

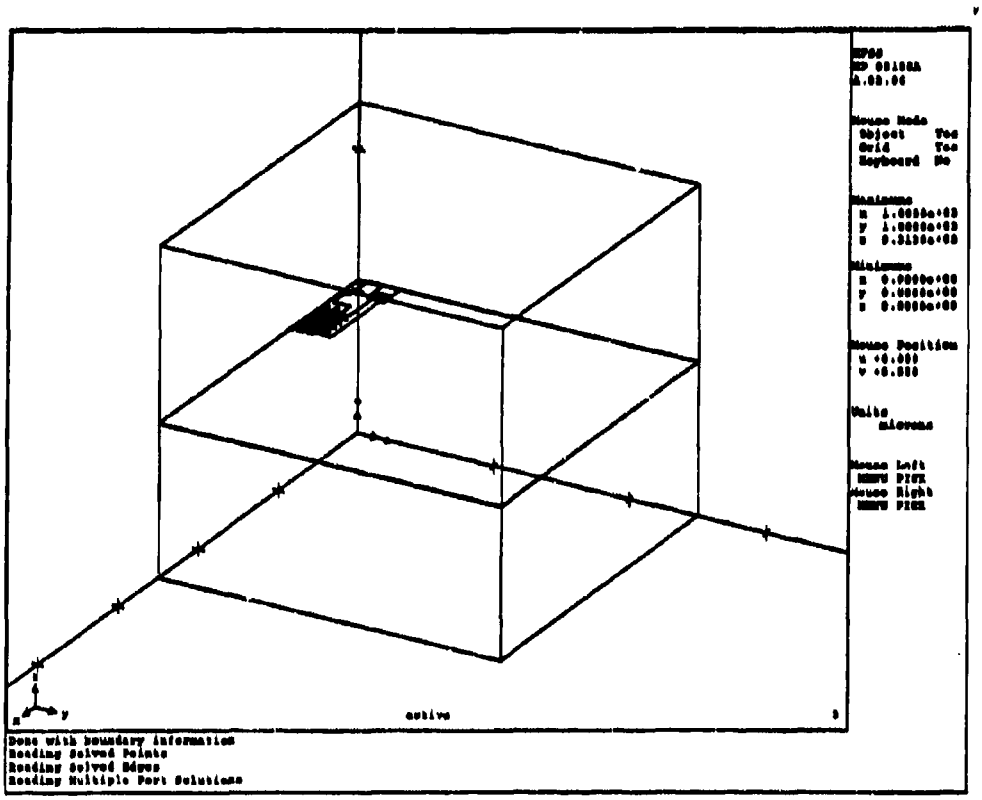

Figure 2-9. Under Dense Structure Simulation - Full View.

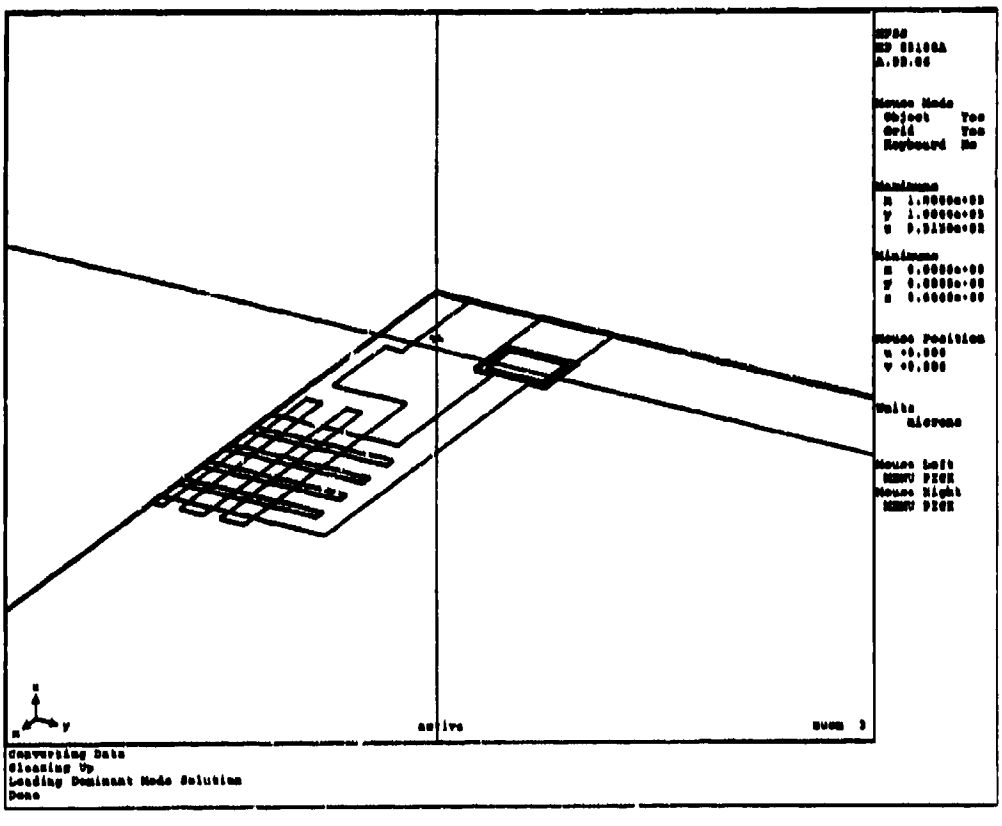

Figure 2-10. Under Dense Structure Simulation - Zoom.

Table 2-1

Structure Capacitance (pF)

	Parallel Plate	Three-Dimensional Simulation	Measured
Dense	0.161	0.221	0.210
Under Dense	0.279	0.871	0.345

2.3 Tip Capacitance

The has been some discussion in the FEA literature of the tip versus the gate metalization capacitance. From our on-wafer measurements of structures with and without tips, the trend is that structures with tips have slightly more capacitance than structures with the hole but without tips. However, a quantitative measurement was not possible because these effects are close to the noise limit of the measuring systems. A quantitative computational result is possible using a two-dimensional R-Theta Poisson solver. Figures 2-11a to 2-11g show the same gate and hole structure with a differing tip height. The r=0 axis is on the right side with the gate metal and the dielectric layer concentric at larger radii. The gate is biased at unity with the solid line showing the potential of one-half. The outer radius of 1.7 microns (3.4 micron diameter) corresponds roughly with the 3 micron rectangular spacing of the actual cathodes. The increasing tip height does cause an increase in capacitance, however, the change is small compared to that of the gate capacitance as shown in Figure 2-12. Also, the one-half gate potential line gets progressively closer to the tip with increasing tip height showing the field enhancement.

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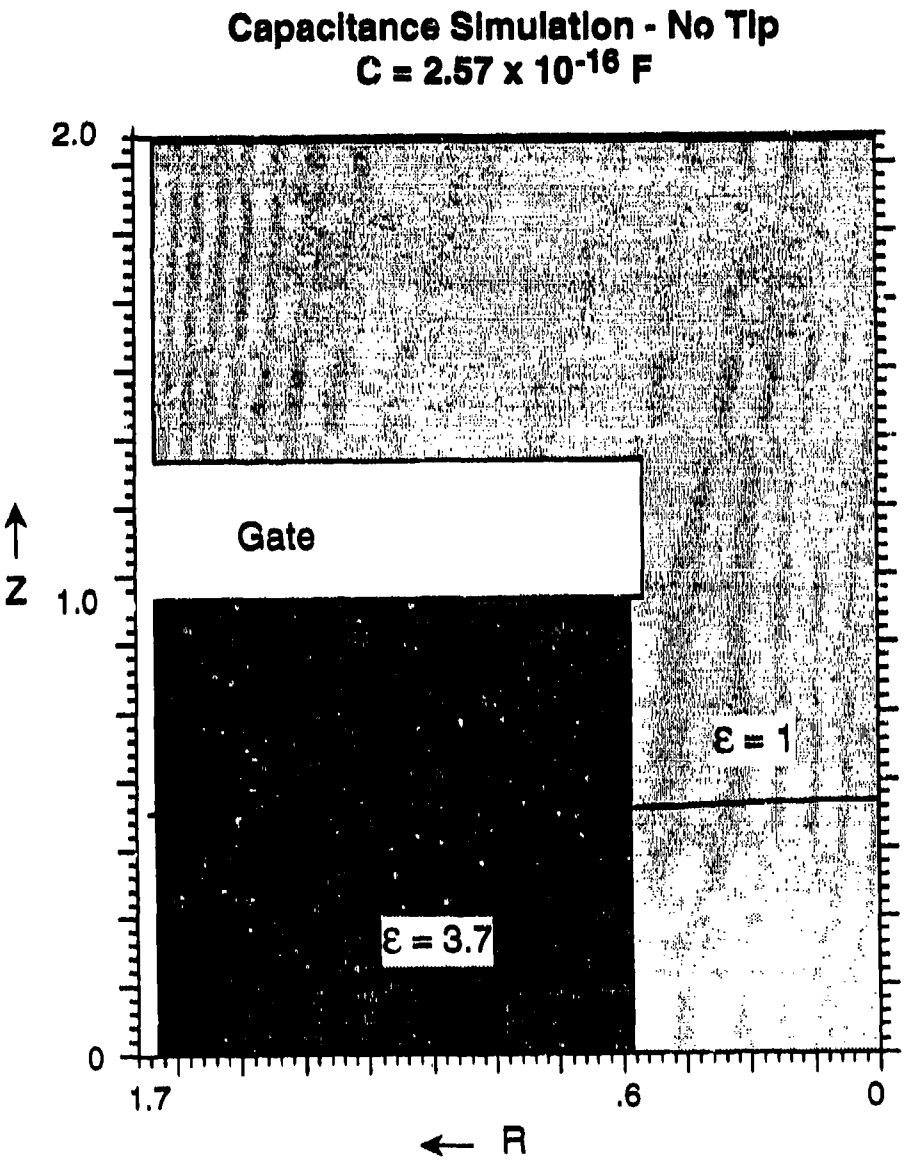

Figure 2-11. (a) Capacitance Simulation Tip Height.

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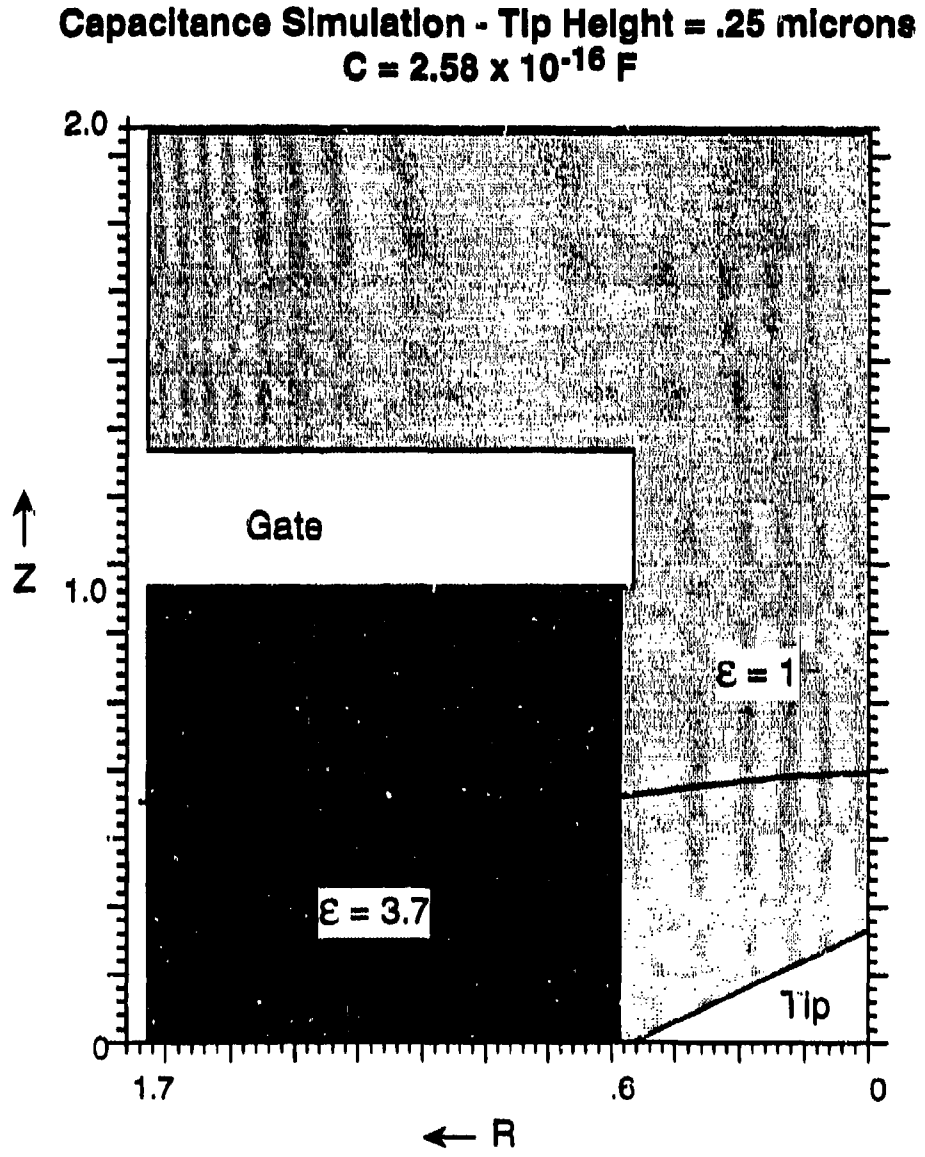

Figure 2-11. (b) Capacitance Simulation Tip Height.

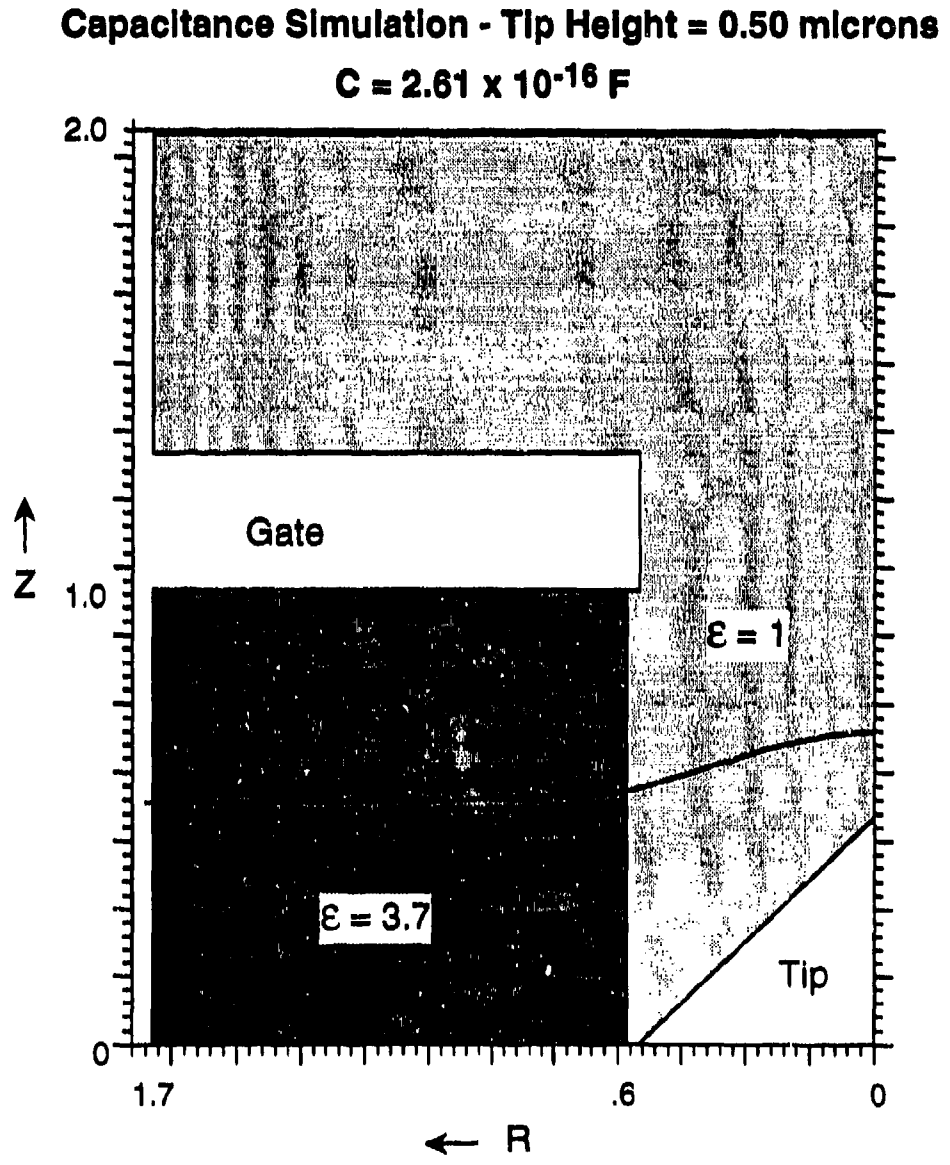

Figure 2-11. (c) Capacitance Simulation Tip Height.

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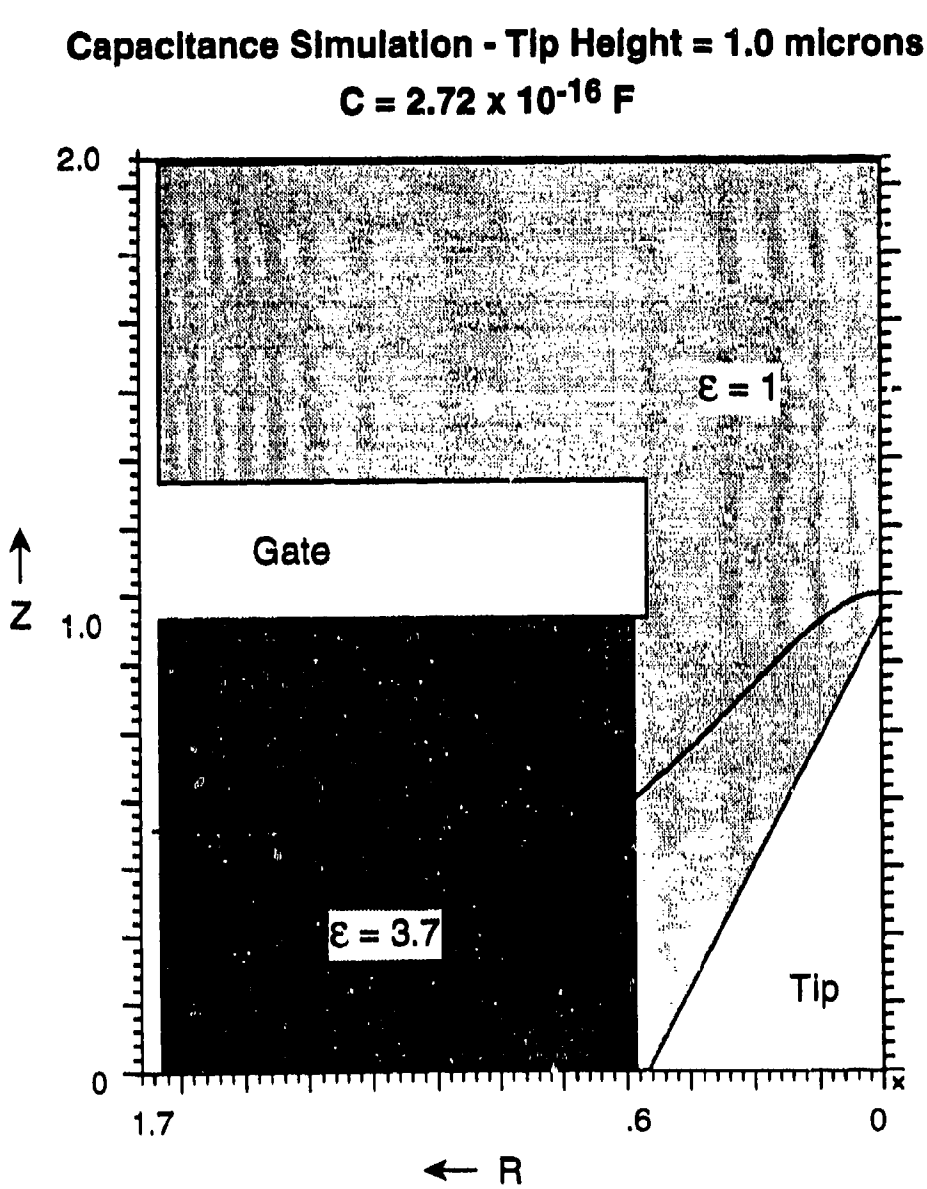

Figure 2-11. (d) Capacitance Simulation Tip Height.

Capacitance Simulation - Tip Height = 1.25 microns

$C = 2.83 \times 10^{-16}$ F

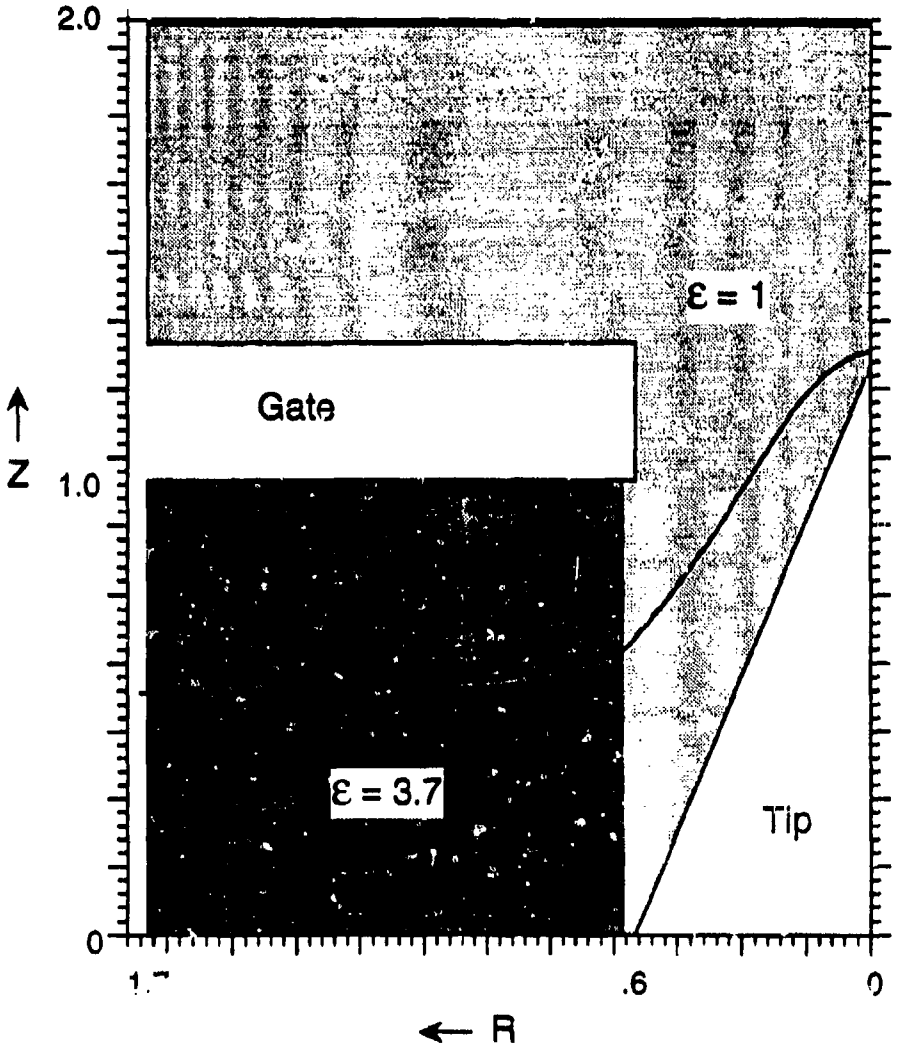

Figure 2-11. (e) Capacitance Simulation Tip Height.

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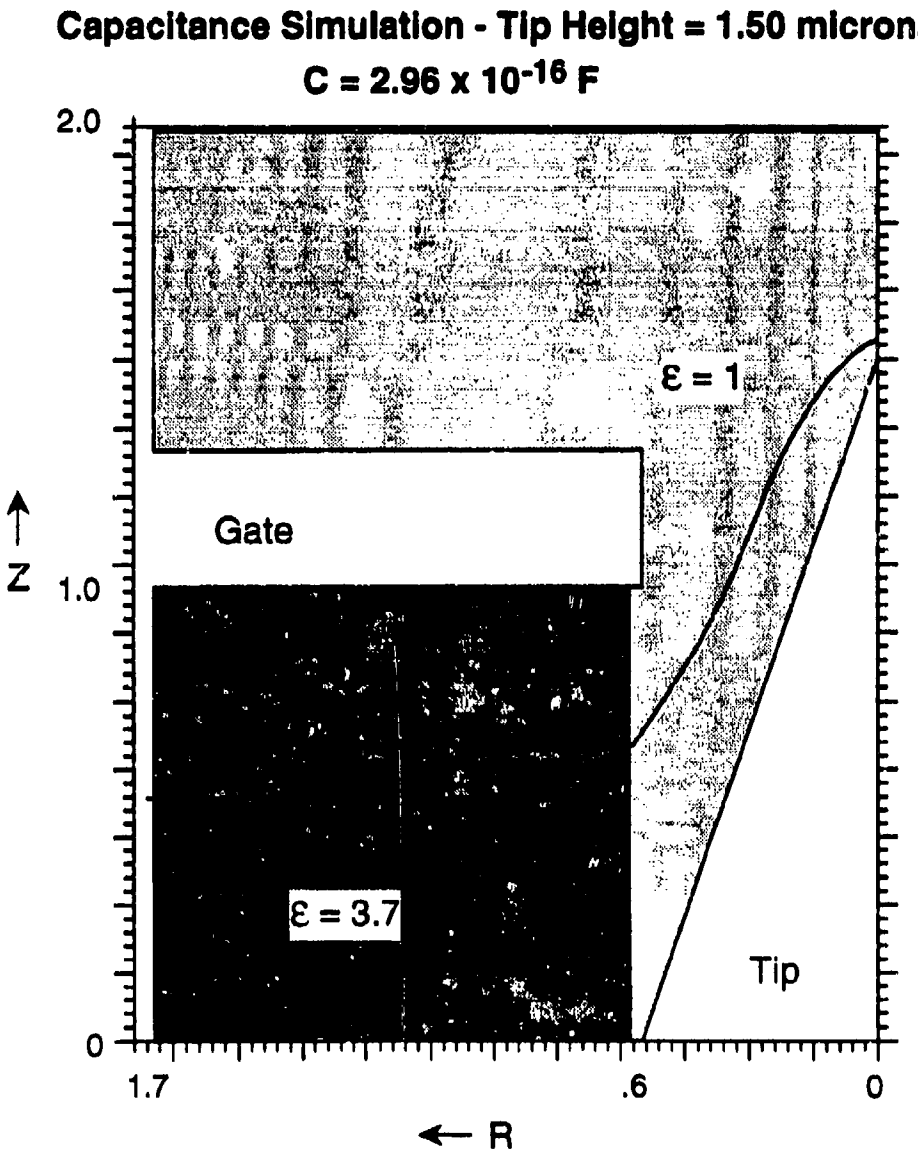

Figure 2-11. (f) Capacitance Simulation Tip Height.

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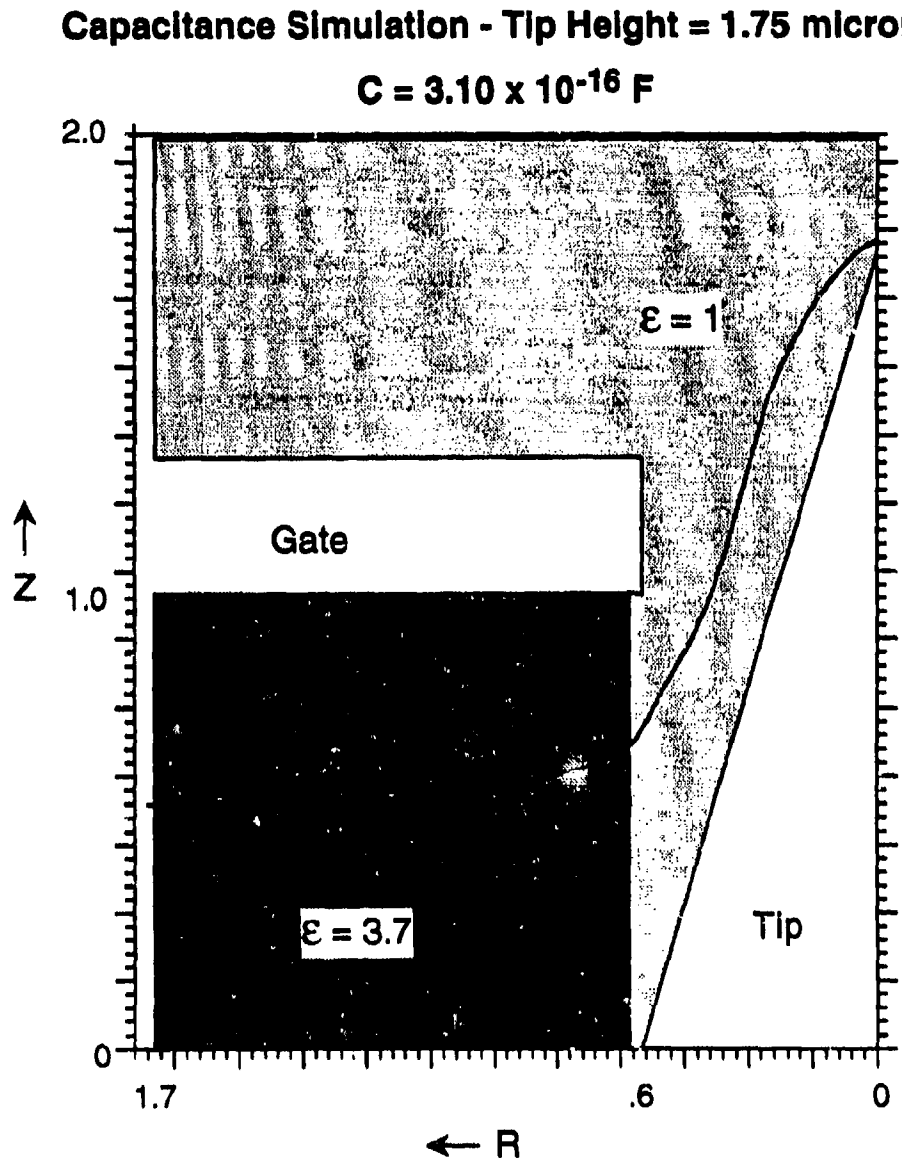

Figure 2-11. (g) Capacitance Simulation Tip Height.

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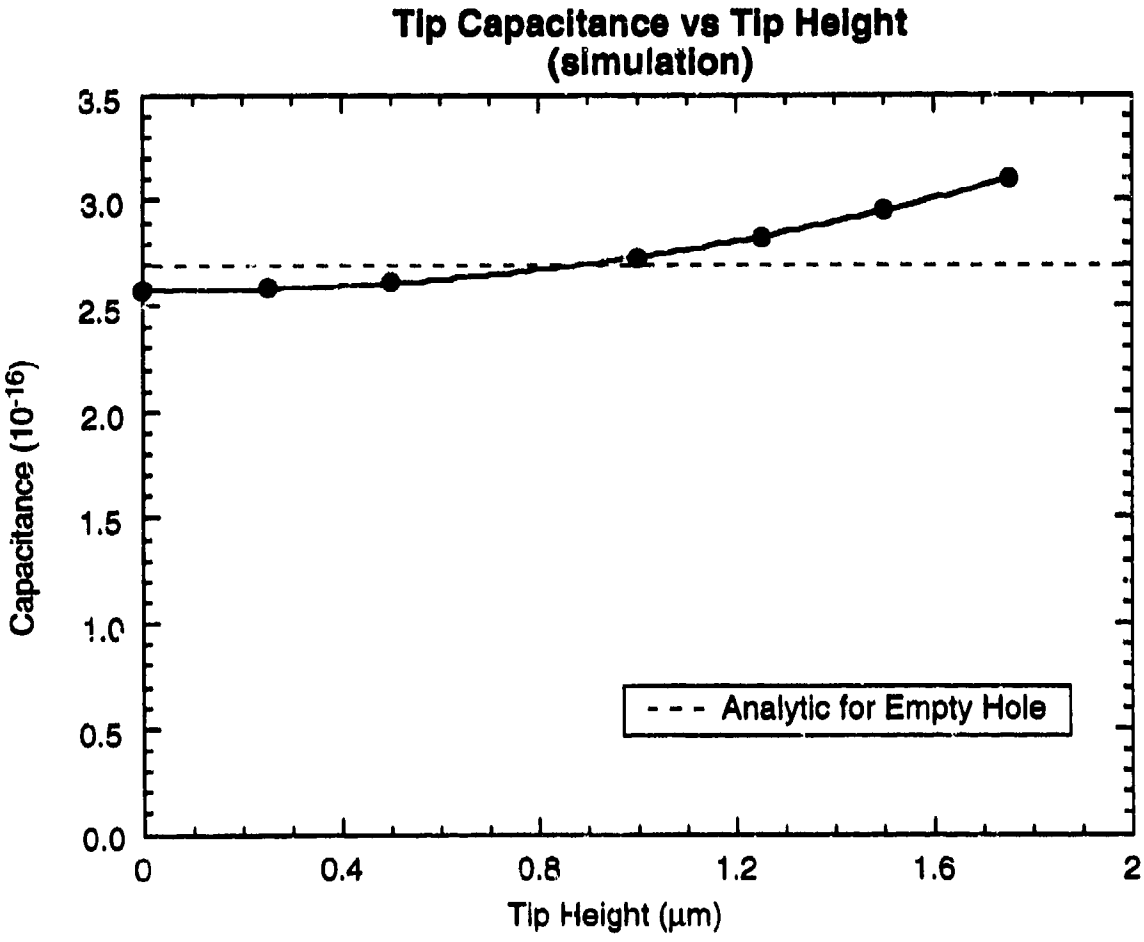


Figure 2-12. Tip Capacitance vs. Tip Height (simulation).

3.0 TEST TRIODES

3.1 Overview

To test these cathodes electrically, it is necessary to bake and test them in ultra-high vacuum. A test station for this purpose has been fabricated under company funds. The device under test is bonded to a ceramic circuit board, which contains metal leads which are wire-bonded to the FEA and, through a vacuum feedthrough, connect to electrical power supplies and RF measuring equipment. The vacuum system is bakable to 450°C. We are also able to test more than one chip at a time.

The pumping system consists of a sorption pump, followed by a turbo pump and then a vac-ion pump. There is no mechanical oil fore-pump in the system. The system is capable of vacuum on the 10^{-10} Torr. There is a residual gas analyzer and a microscope for direct viewing through a window. The power supplies allow operation up to 10 KV although most tests were performed under 2 KV. There is also a moderate voltage (250 volts) gate pulser that allows for low duty operation. Most of the equipment is able to be controlled by a computer. The bakeout sequence, the initial device turn on, and the measurement of I/V characteristics are under program control.

3.2 Alumina

The layout of the third iteration alumina is shown in Figure 3-1 and a photograph in Figure 3-2. There are four tapered grounded co-planar lines. The large size at the edges are compatible with the 0.141" SiO_2 coax lines on the flange while the inner size in compatible with the pitch on the chips. The chip is placed in the milled depression in the center. The depression is the same depth as the height of the chip so when mounted the chip and alumina are flush. The chip and alumina are connected with gold ribbon bonds. The alumina is plated on the backside and the

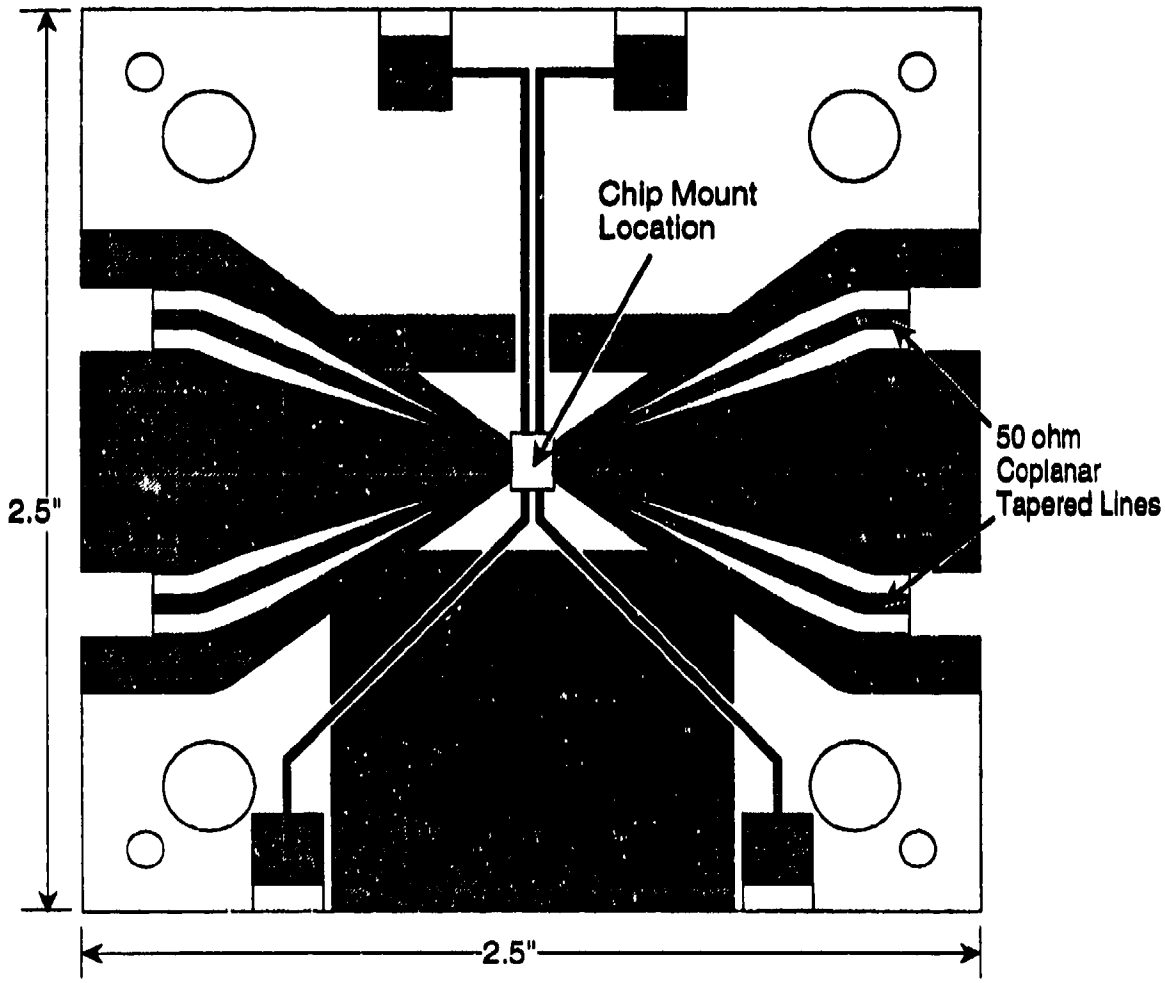


Figure 3-1. Third Iteration FEA Cathode Alumina (layout).

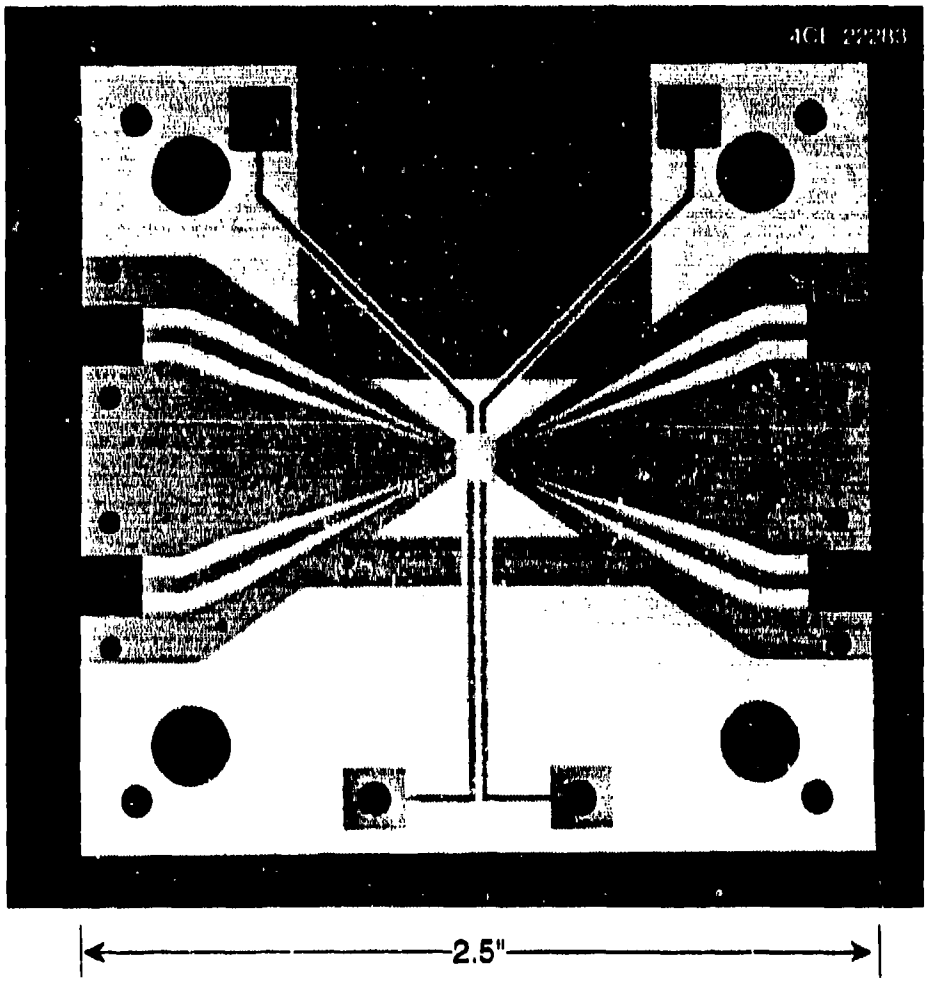


Figure 3-2. FEA Cathode Alumina.

top grounds are connected to the back with through vias. The taper maintains a constant 50 ohms from input to output. The top ground at the bottom is to control the impedance of the anode that cantilevers out over the alumina. The chip has eight cathode connections while the alumina only has four. This is because there is not enough room to fit eight co-planar transitions on the alumina. The vertical pitch on the alumina was twice that of the chip so that the chip could be positioned in the milled depression to connect to four cathodes at a time. There are also four dc leads on the alumina which were planned for control electrodes that were never implemented on the cathodes. Cold testing of these alumina indicated good performance up to 5 GHz.

3.3 Mounting Flange and Anode

A photograph of the alumina mounted in the vacuum flange is shown is Figure 3-3 with a close up in Figure 3-4. The four cathode coax lines are clamped with copper blocks around the outer conductor to the alumina with spring loaded screws. The coax line center conductor is placed on the co-planar center conductor with a piece of indium foil for contact. A heater is placed on the backside of the alumina for bakeout. The anode outer conductor is clamped to the alumina ground in a similar manner to the cathodes. The copper anode lead cantilevers out over the top ground and has clamp at the end. A pre-fired hollow moly anode sits over the cathode. The anode cathode spacing was typically one millimeter. It is desirable to maintain a constant 50 ohm impedance to the moly anode. To optimize this match, a set of alumina sleeves were fabricated to go around the anode lead to adjust the impedance. It turned out that the best match was obtained with no alumina sleeve.

One way to evaluate the match of the anode is to use the time domain feature of a vector network analyzer. Just looking at the reflection coefficient over frequency is not good enough because the reflections might not all be occurring at the same reference plane. Time domain reflectometry gives the position and magnitude

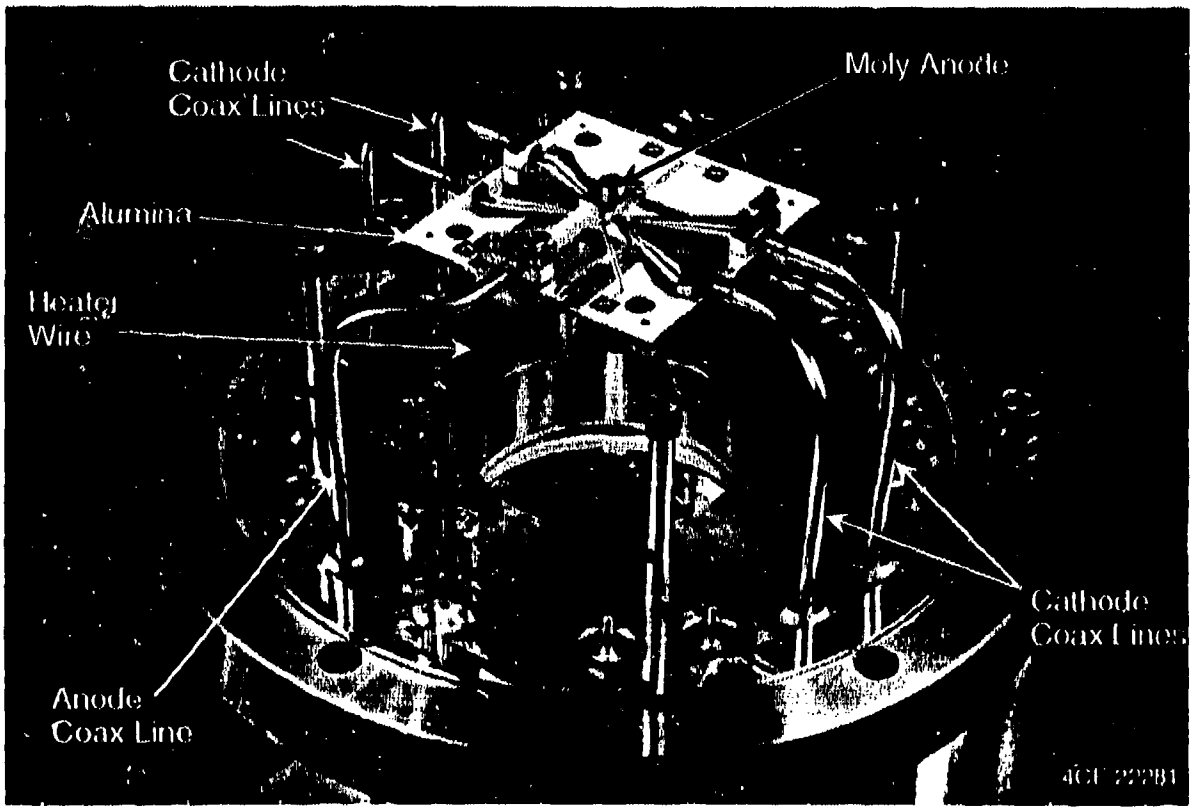


Figure 3-3. FEA Triode Mounted on Test Flange.

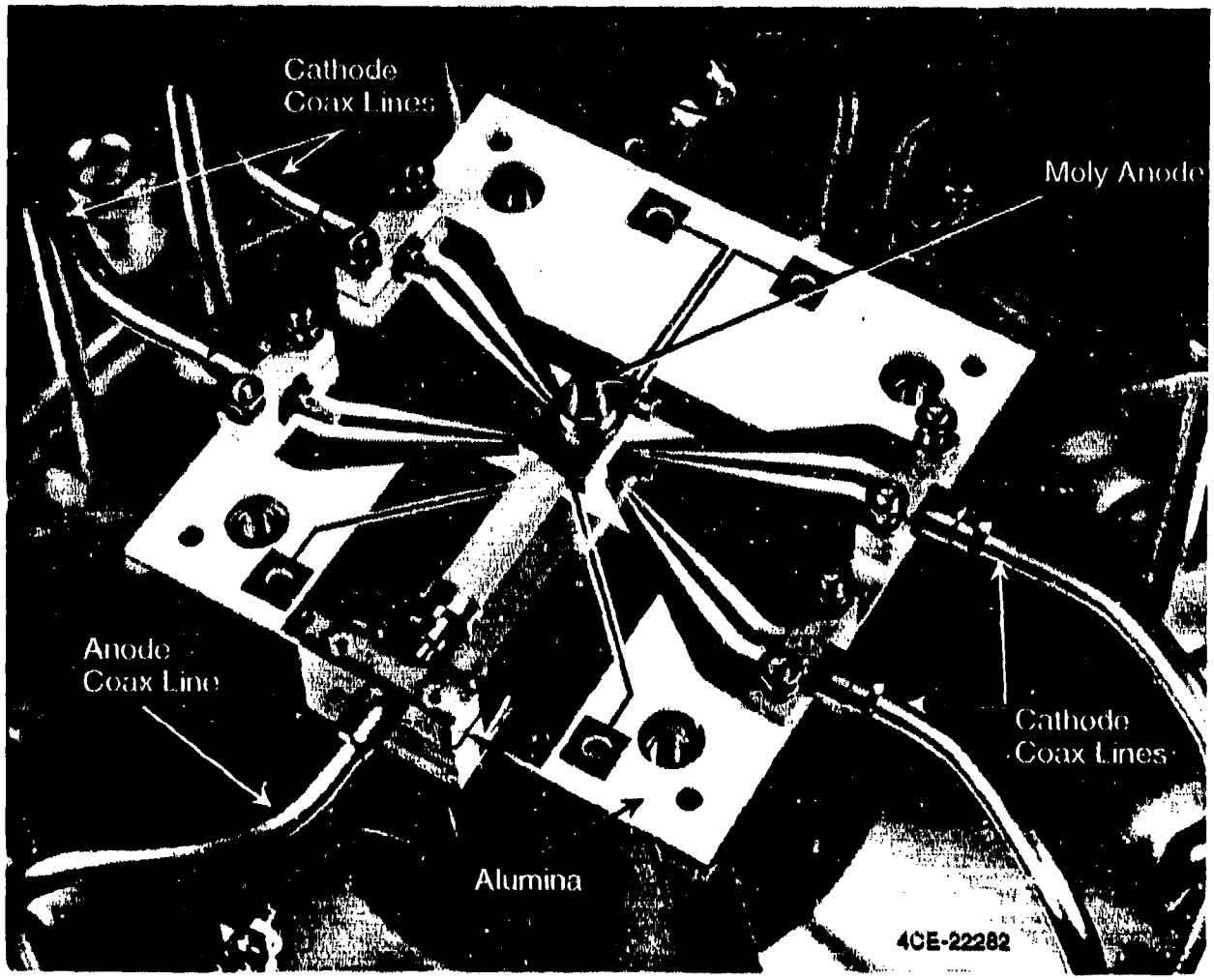


Figure 3-4. FEA Triode (close-up).

of the reflection integrated over frequency. The time domain result with the anode lead removed is shown in Figure 3-5. The average reflection coefficient from 50 MHz to 2.05 GHz is 0.98 and as the figure shows there is a well defined reference plane. The result for the anode is place is shown in Figure 3-6. The reduced amplitude is due to the losses and radiation from the anode. Again there is a well defined single peak that shows that the anode line is well matched until the open circuit at the end.

3.4 Test Configuration and Equivalent Circuit

A block diagram of the test configuration is shown is Figure 3-7. Microwave test equipment operates at 50 ohms and the triode FEA triode impedance is much higher. Therefore tuners are required to transform from 50 ohms to the triode impedance for best operation. However, interpreting the results to obtain a measure of g_m is more complicated.

The source was a HP 8656A synthesizer with maximum frequency of 990 MHz. The source was amplified to provide a one volt peak input and lead through a cable to the tuners. The input to the input tuner and the output of the output tuners are connected through circulators so the source and load are well matched. The tuners are commercial off the shelf items that provide a greater than 10:1 VSWR at 1 GHz. The tuned 3 dB bandwidth is typically 10 MHz. The cathode gate bias and the anode high voltage bias are connected through the center conductors of the RF leads by commercial bias-T's. The high voltage limit on these units were 500 volts. The input and output tuners were connected directly to the FEA flange. The load was a high speed digitizing oscilloscope with a one GHz bandwidth plug-in.

The actual data was taken at reference planes A-H. Since the cables are all 50 ohms and are well matched by the circulators, a simple scalar correction for cable loss transforms to reference plane B-G. Vector correction using the full S-parameters of the

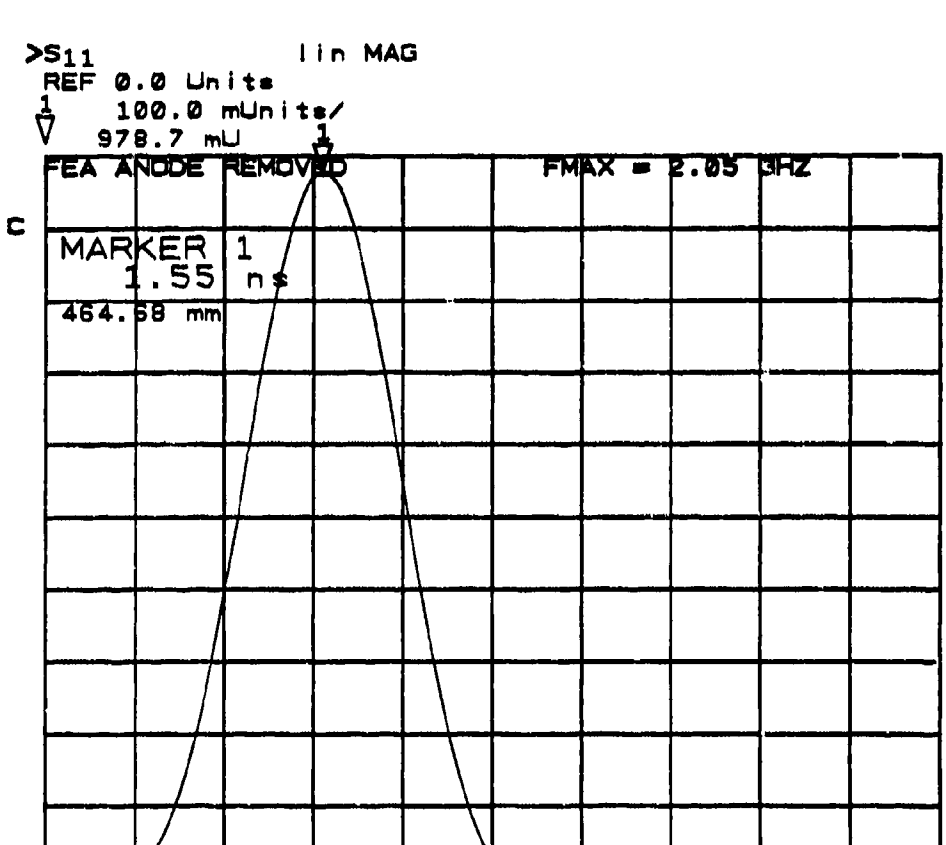


Figure 3-5. Time Domain Analysis of FEA Flange Anode Removed.

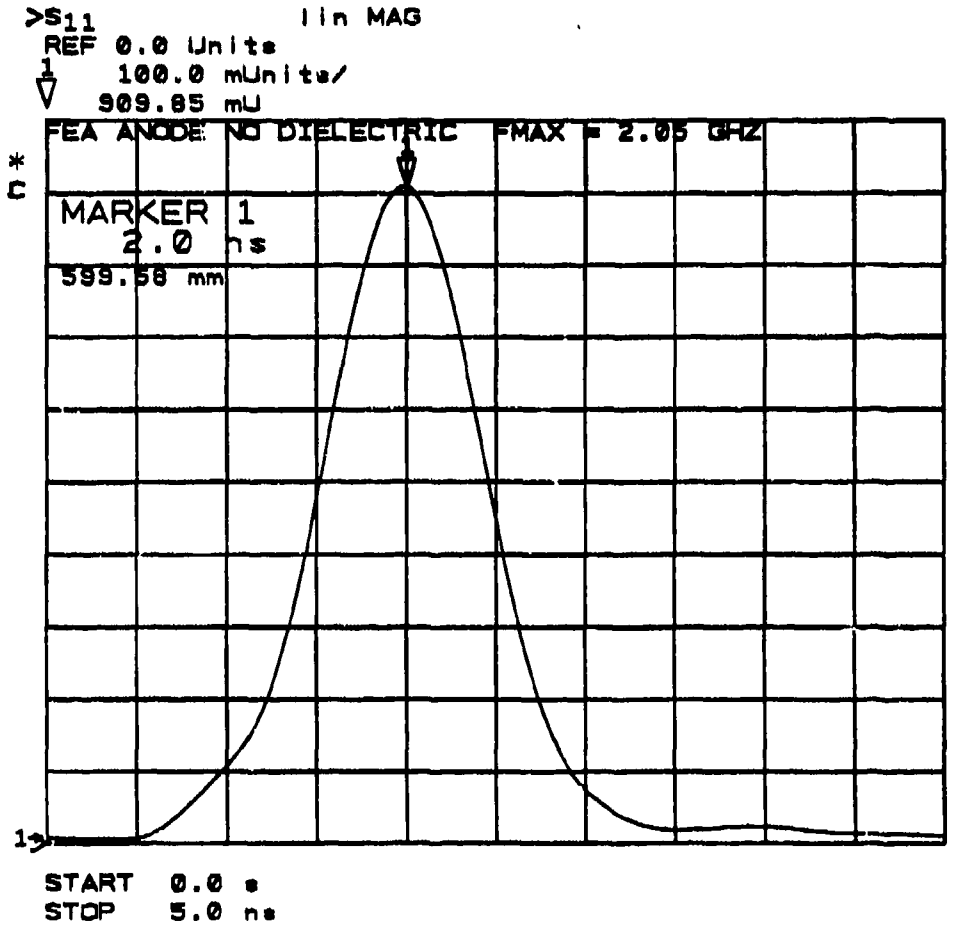
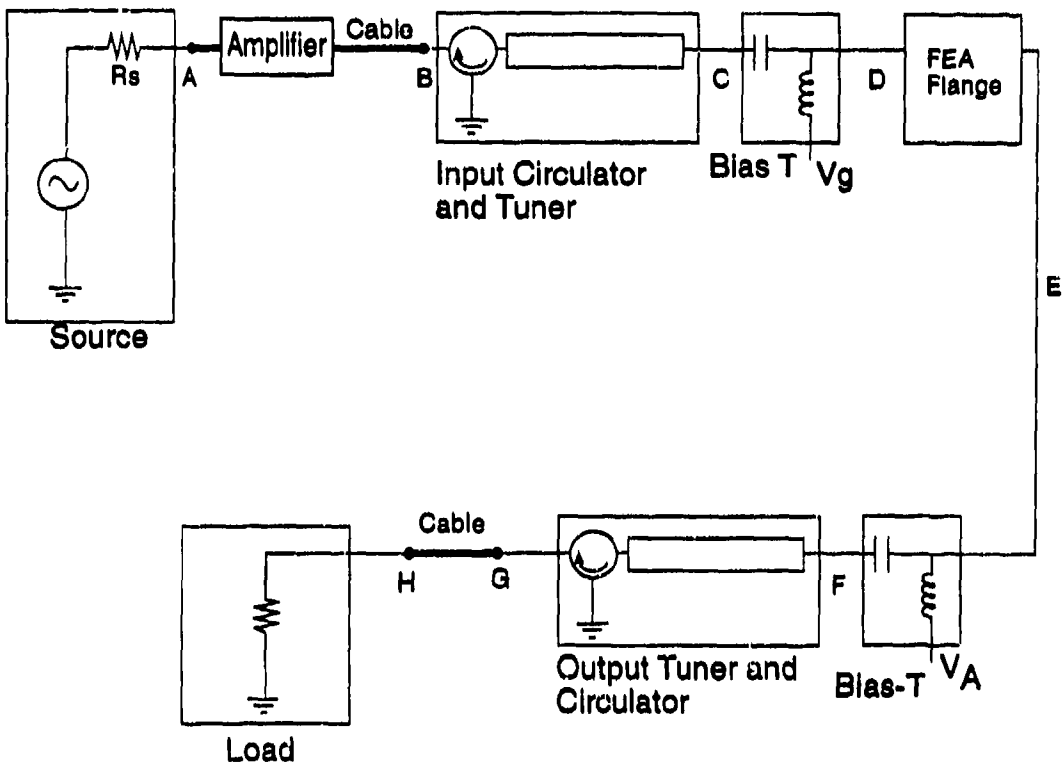


Figure 3-6. Time Domain Analysis of FEA Flange Anode in Place.



Reference Planes

A–H Measurement - tuned
B–G 50 Ω cable loss removed–tuned
C–F Untuned

Conponents

Source	HP 8656A Synthesizer
Amplifier	Avantek APG-2022M
Circulator	Trak 50A1101
Tuner	Microlab/Fxr SF–11F
Bias–T	KDI Triangle EP/8
Load	Tektronix 11403A/11A81 Oscilloscope/Plug-In

Figure 3-7. FEA Triode Test Configuration.

input and output tuners are required to transform to the un-tuned reference plane of C-F.

The FEA triode equivalent circuit is shown in Figure 3-8. The triode is connected in a common cathode configuration. The input transmission line contains the input bias-T, the coax line of the flange, and the co-planar tapered line of the alumina. The output transmission line contains the cantilevered cathode, the coax line of the flange, and the output bias-T. The value of the gate capacitance C_g was obtained by on-wafer probing of a single chip. The values of the other cold circuit values were obtained by measuring the full S-parameters at the C-F reference plane and fitting. The model was not very sensitive to the value of C_A.

The tuners were attached and the system was tuned for the highest value of S_{21} (transmission). They were then removed and measured individually. The results are summarized in Table 3-1. The condition of conjugate match is equivalent magnitude and opposite sign of the angle and is expected for best internal match at a high VSWR interface. As can be seen by the S-parameters of both the output match of the input tuner and the input match of the un-tuned circuit and the input match of the output tuner and the output match of the un-tuned circuit, this conjugate match condition is met (solid lines in Table 3-1).

3.5 Test Results

Many triodes were mounted and tested. Most of the tests were run with one millisecond pulse widths, four percent duty, and 500 volts on the anode. The current was slowly increased over a period of many hours. A level of 400 microamps was routinely obtained (1 μA/tip) while higher currents were not that common. Our best result of 7.3 milliamps is presented in detail.

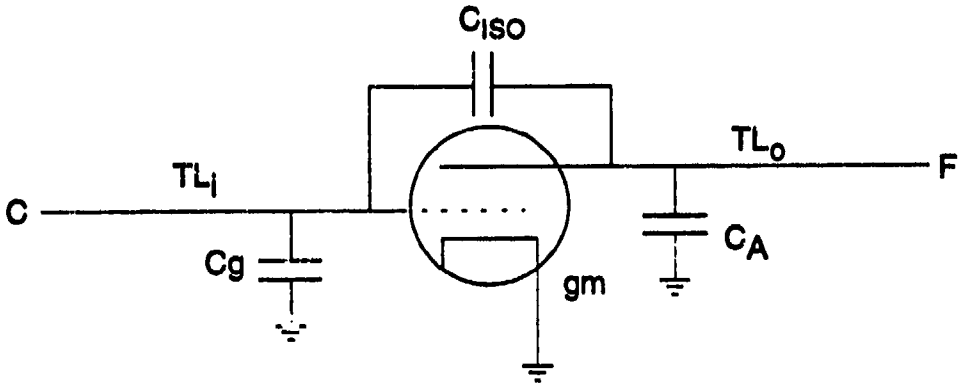
The oscilloscope traces are shown in Figure 3-9. The voltage and current are straightforward traces. The microwave trace is

Table 3-1

S-parameters of Flange/Tuners at 990 MHz

PBN-94-1890

	S11		S21		S12		S22	
	Mag	Angle	Mag	Angle	Mag	Angle	Mag	Angle
Tuned B–G	.051	79.7	.047	104.8	1.9×10^{-4}	-16.7	.118	3.6
Un-Tuned C–F	.818	-38.7	.012	79.4	.012	79.3	.946	-168.0
Input Tuner B–C	0.55	12.8	.483	91.9	.067	-13.7	.849	39.2
Output Tuner F–G	.946	167.5	.290	95.7	.008	-66.1	.102	-.01
Equivalent Circuit B–G	.136		.051		2.2×10^{-4}		.087	
Equivalent Circuit C–F	.817		.014		.014		.946	



TL_i = Input transmission line
Electrical Length = 61.59 cm
Loss (db/cm) = .0060
Total Loss (50Ω) = .37 dB

TL_o = Output transmission line
Electrical Length = 67.57 cm
Loss (db/cm) = .0036
Total Loss (50Ω) = .24 dB

C_g = Gate Capacitance
= .345 pF
Q = 1.80
R = 258Ω

C_A = Anode Capacitance
= .010 pF

C_{ISO} = Isolation Capacitance
= .026 pF

g_m = Transductance

Figure 3-8. FEA Triode Flange Equivalent Circuit.

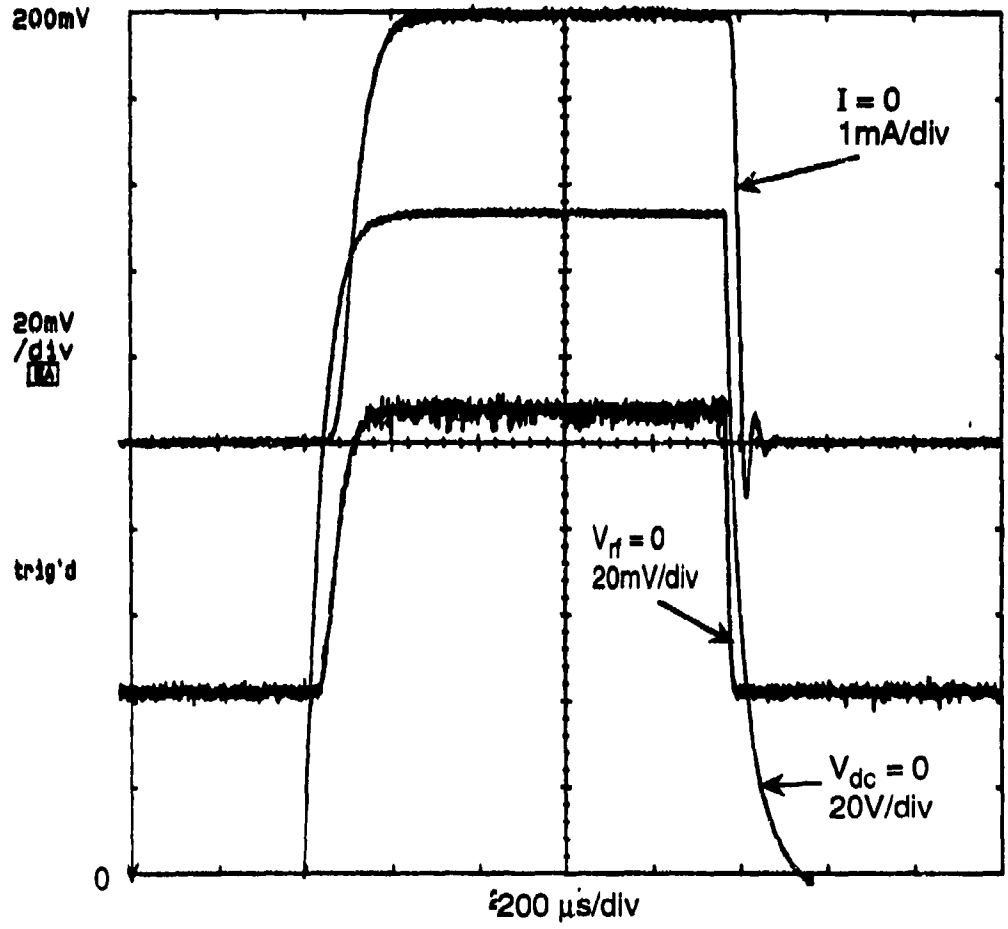


Figure 3-9. FEA Triode I-V and Microwave Traces.

processed by the scope. The signal is the envelope of the averaged signal. This gives a rectified peak reading over the pulse. The input value was set at 1 volt.

The I-V results are shown in Figure 3-10 and shows the typical exponential dependence of the current on the voltage. Table 3-2 summarizes the measured and derived quantities. The first three columns are the raw data of current, gate voltage, and RF amplitude. The dc g_m and F_t are calculated from the I-V data and tabulated. The RF amplitude is converted to dB insertion loss and then corrected for the cable loss (Figure 3-11). From this data, a g_m is derived.

The equivalent circuit of the flange/bias-T is cascaded on a circuit simulator with the measured input and output tuner S-parameters. The g_m of the circuit is adjusted so that the S_{21} agrees with the measured data. These results are tabulated under g_m RF. From this value of g_m RF, the final value of F_t RF is calculated. This yields a maximum measured F_t of 201 MHz. A composite of the dc and RF g_m is plotted in Figure 3-12 and the dc and RF F_t in Figure 3-13. As expected the two sets of derived quantities track closely. The measured and equivalent S-parameters at the peak current are listed in the S_{21} column of Table 3-1. Since the measurements were performed at a frequency greater than F_t, there is no gain, only reduced insertion loss.

The tuners were readjusted under hot conditions to see if there were any load-pull improvements. The hot tuning and cold tuning were identical which is not unexpected since the device with no gain is running in a small signal regime. Also, it was not possible to perform a reliable noise figure measurement with such a high insertion loss.

Table 3-2

Table of Measured Data for 2T39-6.7.54

PBN-94-1876A

V_{rf} in = 1V
C = .345 pf
$f_t = gm/2\pi C$
Cable Loss = 1.54 dB

V_{annode} = 500V
PW = 1 mS
Duty = 4%

	I	V_{dc}	V_{rf} out	gm dc	Ft dc	G@cab	G@Tun	gm RF	Ft RF
1	7.3e-03	154.00	1.47e-01	5.1e-04	2.35e+08	-16.65	-15.11	4.36e-04	2.01e+08
2	4.0e-03	146.00	1.04e-01	3.1e-04	1.42e+08	-19.66	-18.12	2.90e-04	1.34e+08
3	3.0e-03	143.00	9.60e-02	2.4e-04	1.11e+08	-20.35	-18.81	2.50e-04	1.15e+08
4	2.5e-03	140.00	8.90e-02	2.1e-04	9.61e+07	-21.01	-19.47	2.10e-04	9.69e+07
5	2.0e-03	137.00	8.15e-02	1.7e-04	8.00e+07	-21.78	-20.24	1.80e-04	8.30e+07
6	1.5e-03	135.00	7.35e-02	1.3e-04	6.17e+07	-22.67	-21.13	1.50e-04	6.92e+07
7	1.2e-03	134.00	6.95e-02	1.1e-04	5.00e+07	-23.16	-21.62	1.40e-04	6.46e+07
8	1.0e-03	131.50	6.50e-02	9.4e-05	4.31e+07	-23.74	-22.20	1.10e-04	5.07e+07
9	8.0e-04	130.00	6.10e-02	7.6e-05	3.52e+07	-24.29	-22.75	1.00e-04	4.61e+07
10	6.5e-04	129.00	5.9e-02	6.3e-05	2.90e+07	-24.58	-23.04	9.00e-05	4.15e+07
11	5.0e-04	126.50	5.50e-02	5.0e-05	2.32e+07	-25.19	-23.65	7.00e-05	3.23e+07
12	4.0e-04	123.00	5.30e-02	4.2e-05	1.95e+07	-25.51	-23.97	5.00e-05	2.31e+07
13	3.0e-04	120.00	5.00e-02	3.3e-05	1.53e+07	-26.02	-24.48		
14	2.5e-04	118.50	4.85e-02	2.8e-05	1.31e+07	-26.29	-24.75		
15	2.0e-04	116.00	4.78e-02	2.4e-05	1.09e+07	-26.41	-24.87		
16	1.5e-04	113.50	4.63e-02	1.8e-05	8.49e+06	-26.69	-25.15		
17	1.3e-04	112.50	4.55e-02	1.6e-05	7.19e+06	-26.84	-25.30		
18	1.0e-04	110.00	4.50e-02	1.3e-05	6.00e+06	-26.94	-25.40		
19	8.0e-05	108.20	4.40e-02	1.1e-05	4.95e+06	-27.13	-25.59		
20	6.5e-05	107.00	4.35e-02	8.9e-06	4.11e+06	-27.23	-25.69		
21	5.0e-05	105.00	4.30e-02	7.1e-06	3.27e+06	-27.33	-25.79		
22	4.0e-05	103.50	4.23e-02	5.8e-06	2.69e+06	-27.47	-25.93		
23	3.0e-05	101.00	4.20e-02	.6e-06	2.11e-06	-27.47	-26.93		
24	2.5e-05	100.00	4.17e-02	3.9e-06	1.79e+06	-27.60	-26.06		
25	2.0e-05	98.500	4.15e-02	3.2e-06	1.47e+06	-27.64	-26.10		

PBN-94-1872

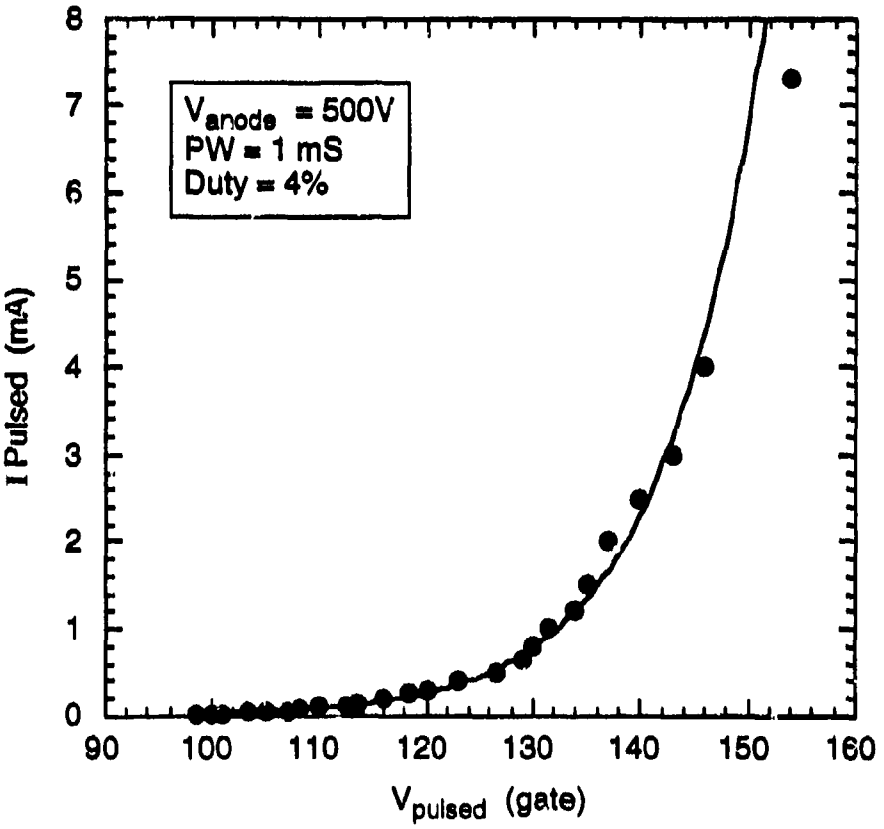


Figure 3-10. I-V of Device 2T39-6.7.S.4.

PBN-94-1874A

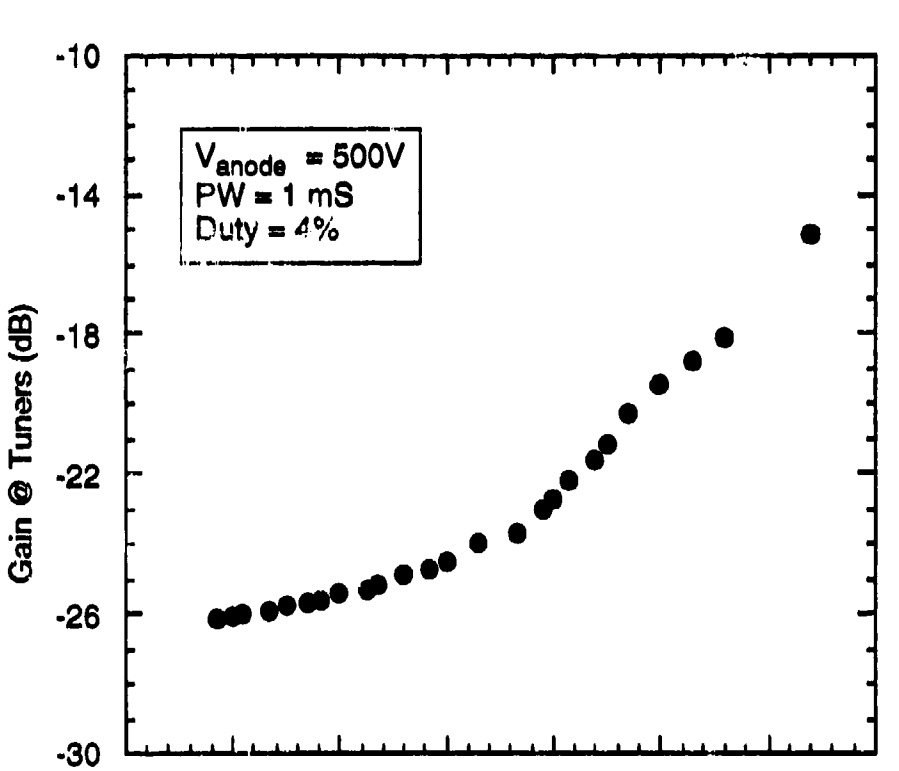


Figure 3-11. Gain at Tuners of Device 2T39-6.7.S.4.

PBN-94-1873

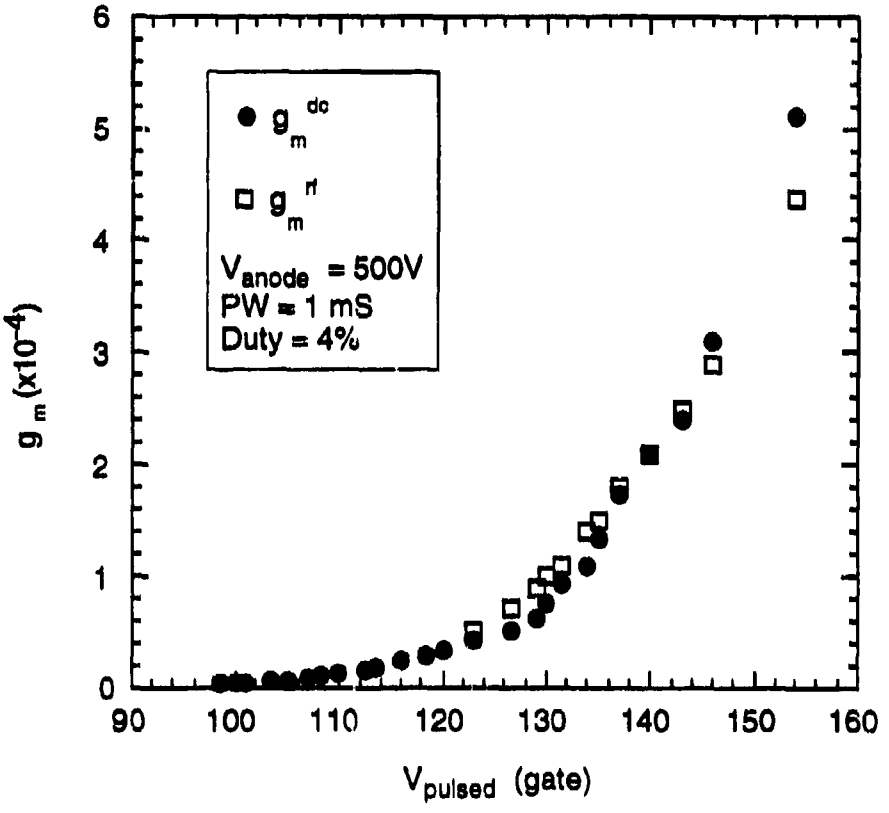


Figure 3-12. Transconductance of Device 2T39-6.7.S.4.

PBN-94-1874

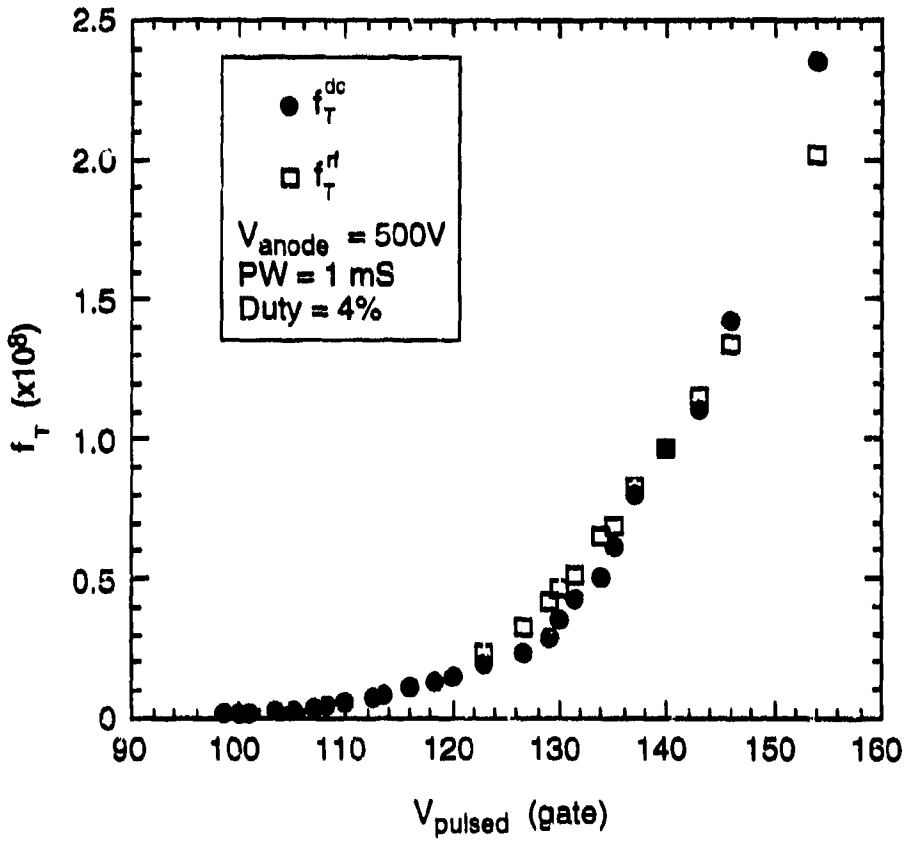


Figure 3-13. Cutoff Frequency of Device 2T39-6.7.S.4.

4.0 COATING EXPERIMENTS

Attempts were made to lower the work function of tips by coating them with carbides. The deposition technique was Pulsed Laser Deposition (PLD). A thin coating (a few molecular monolayers) of hafnium and zirconium carbide were deposited after the the tips were fully formed. No improvements seen in electrical performance. The second approach was to form the last 15% of the tip (~0.15 micron) by PLD. This was tried with hafnium carbide and again there was no improvement in electrical performance.

5.0 CONCLUSIONS

As shown in the body of this report, three of the four goals were met. The most difficult goal was F_t and our best results are still an order of magnitude too low. For operation at 10 GHz, they are two orders of magnitude too low. To meet this goal both an increase in the transconductance g_m and a decrease in gate capacitance C_g are desired. By the nature of the tip formation, there is no obvious way to decrease the gate capacitance. For the Fowler-Nordheim emission that characterizes these cathodes, there are two ways to increase g_m. The first is to increase the current, since to first order g_m scales with current. The problem is that there is a current limit above which the cathodes self-destruct and anode dissipation becomes a problem. The approach of breaking up the dense cathode into a set of sub-cathodes improved the maximum current, however, the improvement was not enough to meet the goals. The second approach is to decrease the gate voltage and our coating experiments were not successful.

Even with a device with a measured dc F_t at 1 GHz, it will be hard to get true power gain at frequency as a triode. These triodes are relatively high impedance devices compared to the standard 50 ohm environment. The dc impedance which is an indicator of the RF impedance is just the inverse of g_m which for a target device is about 1000 ohms. The input must be transformed up and the output must be transformed down. However, operation at the high impedance will enhance the deleterious effect of the gate to anode capacitance. This impedance problem is not as bad for a gated cathode application as for triode operation.

It is not clear after all this investigation that gated field emission cathodes will ever operate in the microwave regime.